

Report
on

“2181” ALU PROJECT

designed for

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designed by

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*ECGR 2181 - Section 001
Logic System Design I*

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PREFACE

It was a responsibility of Paolo Batoni to design an Arithmetic Logic Unit (ALU) with three A inputs, three B inputs, three S inputs, four D outputs, one G output, and one E output, by solely using what was learned during the length of the Logic System Design I taught by Rafic M. Makki, PhD, at the Department of Electrical and Computer Engineering Science of the University of North Carolina at Charlotte.

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INTRODUCTION

Paolo Batoni was requested to design an Arithmetic Logic Unit (ALU) with three A inputs, three B inputs, three S inputs, four D outputs, one G output, and one E output, by solely using what was learned during the length of the Logic System Design I taught by Rafic M. Makki, PhD, at the Department of Electrical and Computer Engineering Science of the University of North Carolina at Charlotte.

For a better visualization of the goal of the project, the general schematics of the above-mentioned ALU was shown in Figure 1, while the operations processed by the logic circuit were enlisted in Table 1.

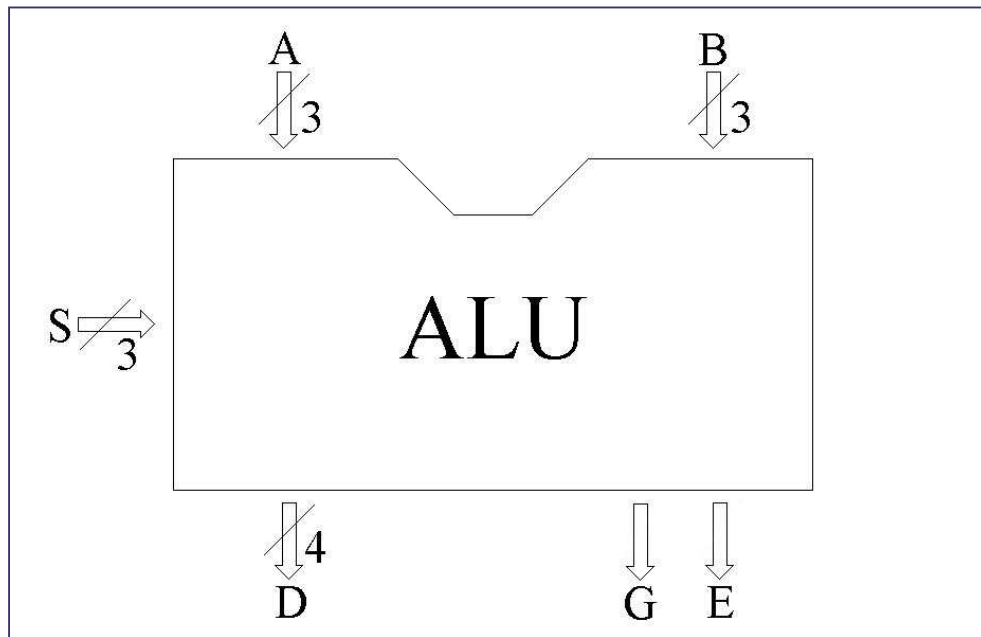


Figure 1: General Schematics of the “2181” ALU

Table 1 Functions and Outputs										
S ₂	S ₁	S ₀	Input		Function	Output	Function	Output	Function	Output
0	0	0	A	B	A + B	D	A > B	G	A = B	E
0	0	1			A - B					
0	1	0			A ⊕ B					
0	1	1			A'					
1	0	0			B'					
1	0	1			0001					
1	1	0			2'S of A					
1	1	1			A NAND B					

For a better comprehension of how the input and the out were processed by the “2181” ALU, a detailed schematics were shown in Figure 2.

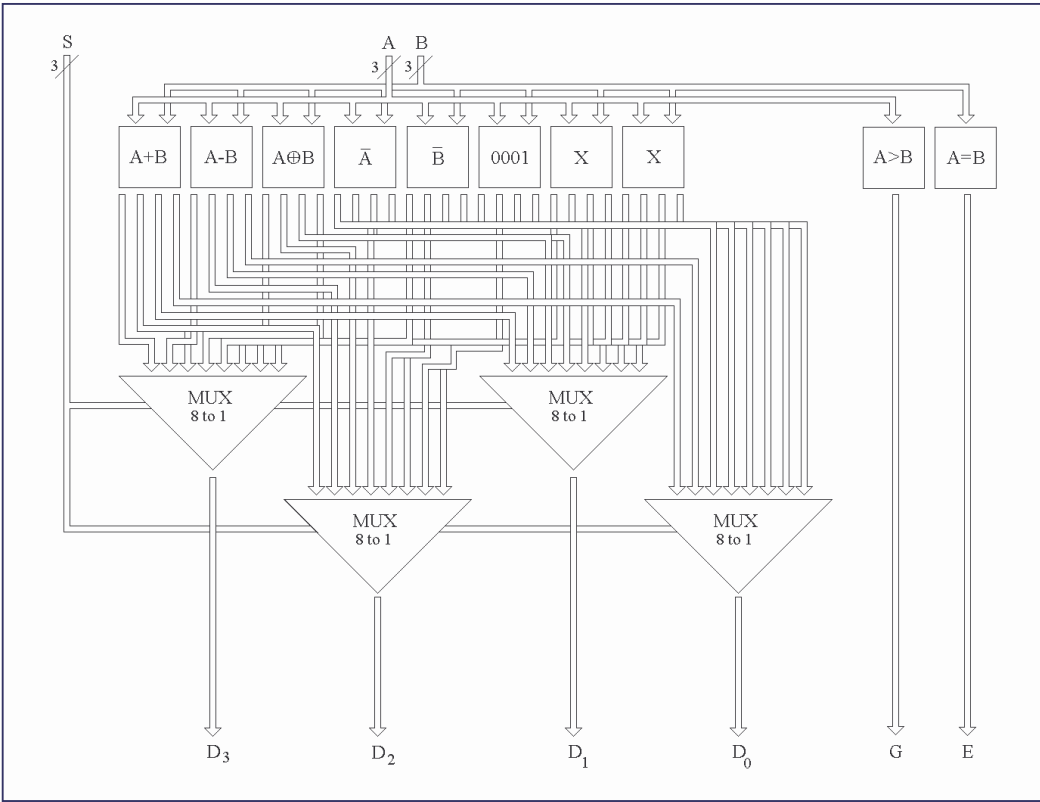


Figure 2: Detailed Schematics of the “2181” ALU

"2181" ALU CIRCUIT DIAGRAM

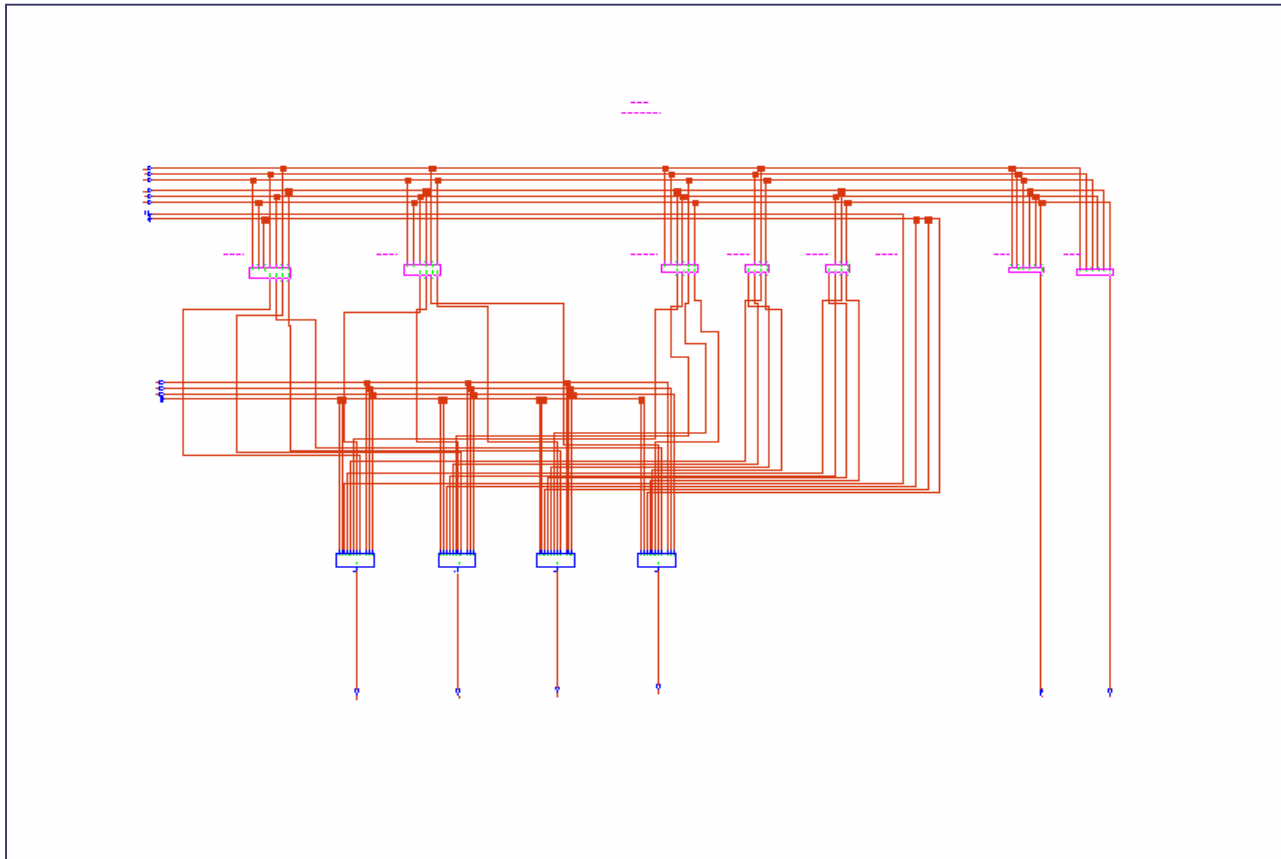


Figure 3: "2181" ALU Circuit Diagram

FUNCTION A + B: Block Diagram

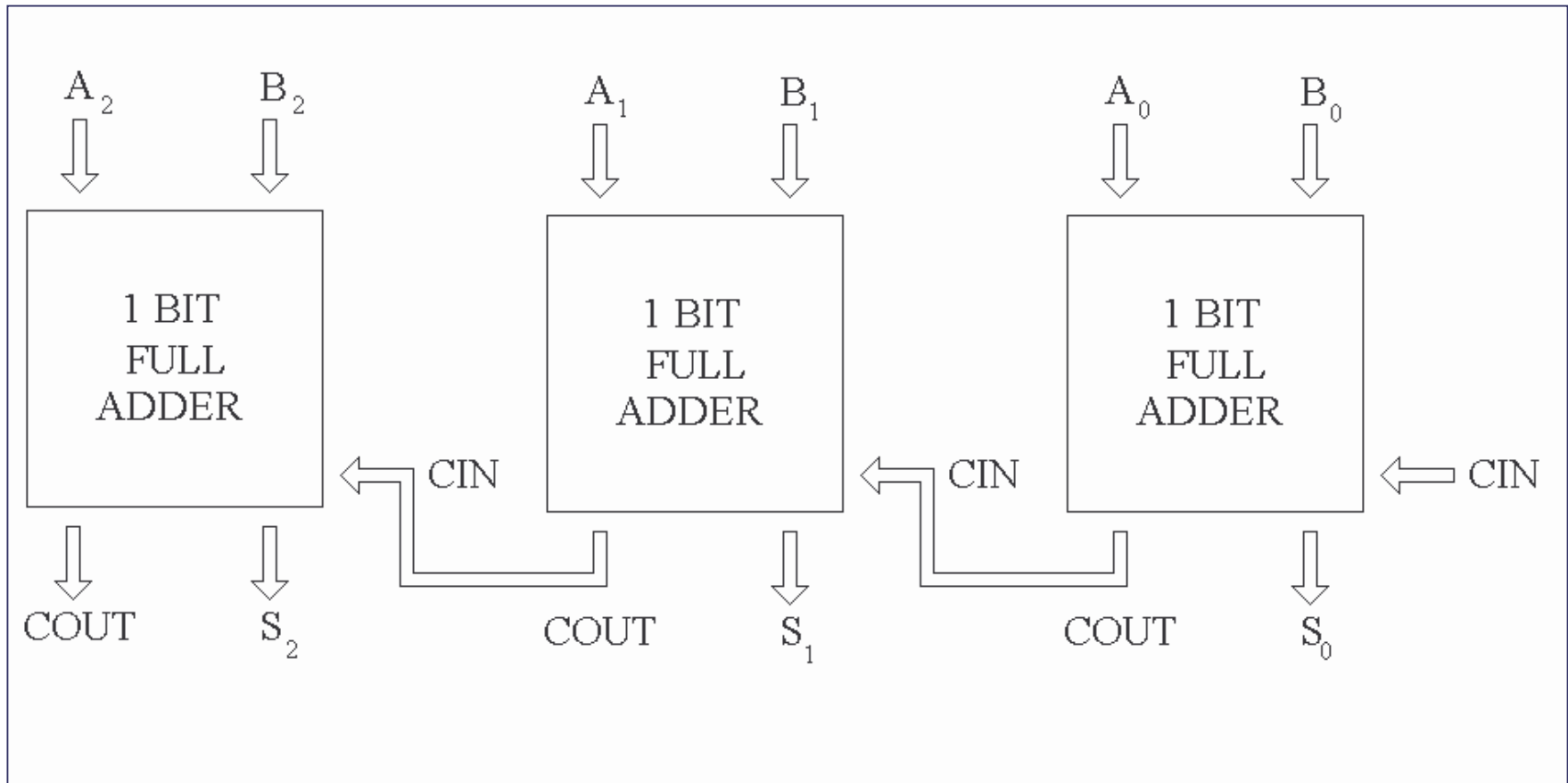


Figure 4: Function A+B Block Diagram

FUNCTION A + B: Modulus Schematics

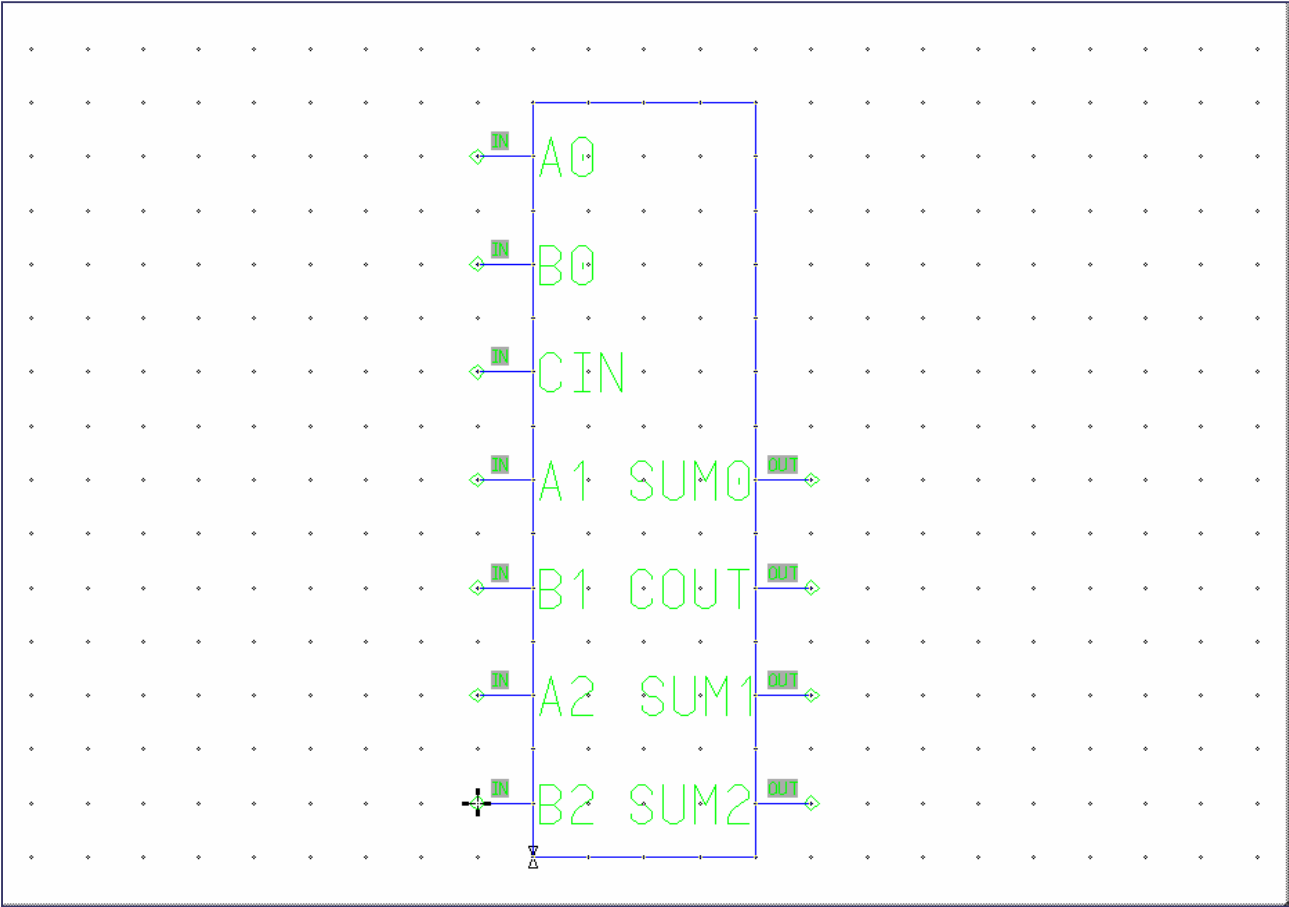


Figure 5: Function A+B Modulus Schematics

FUNCTION A+B: Modulus Circuit

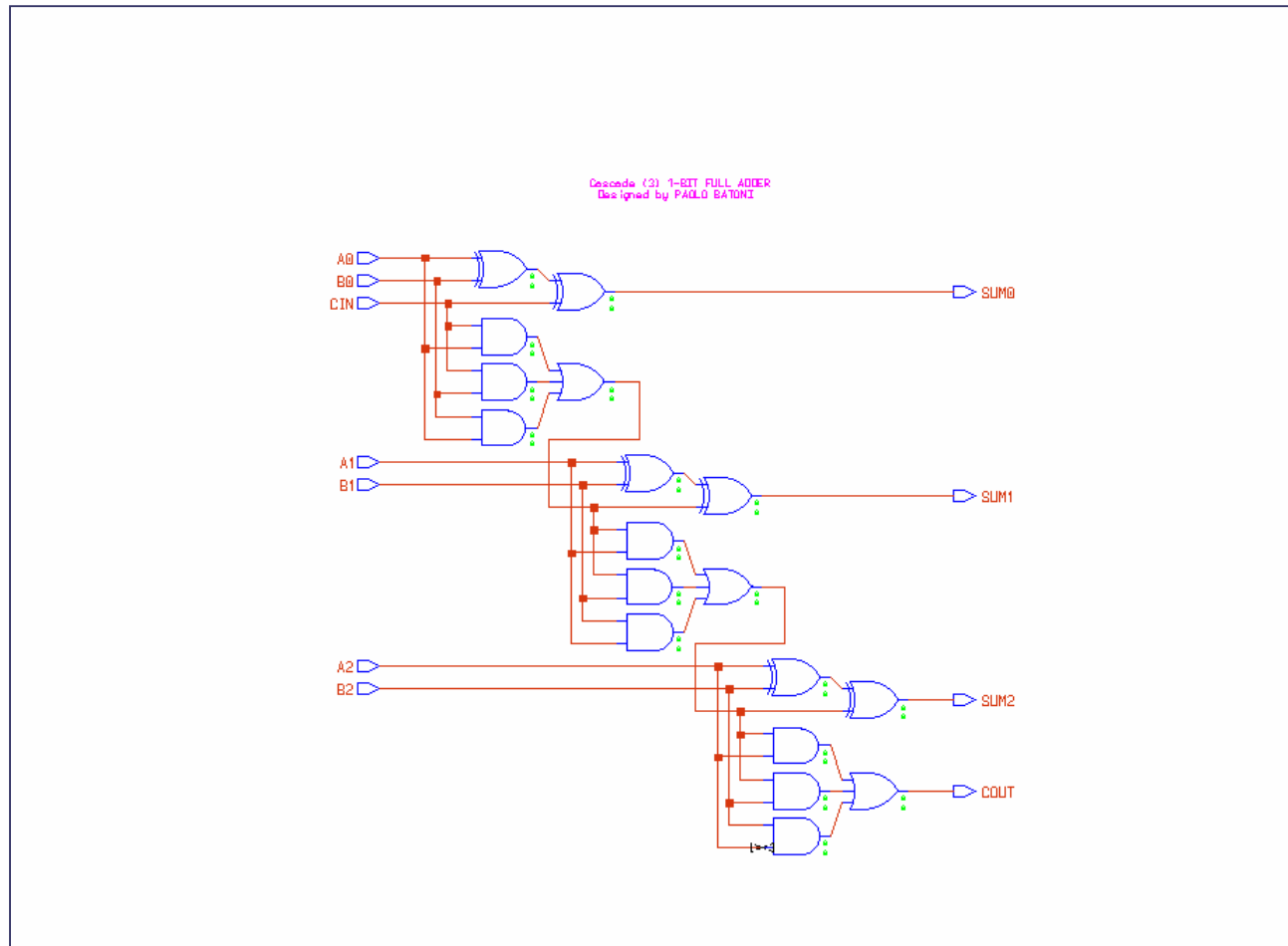


Figure 6: Function A+B Modulus Circuit

FUNCTION A - B: Block Diagram

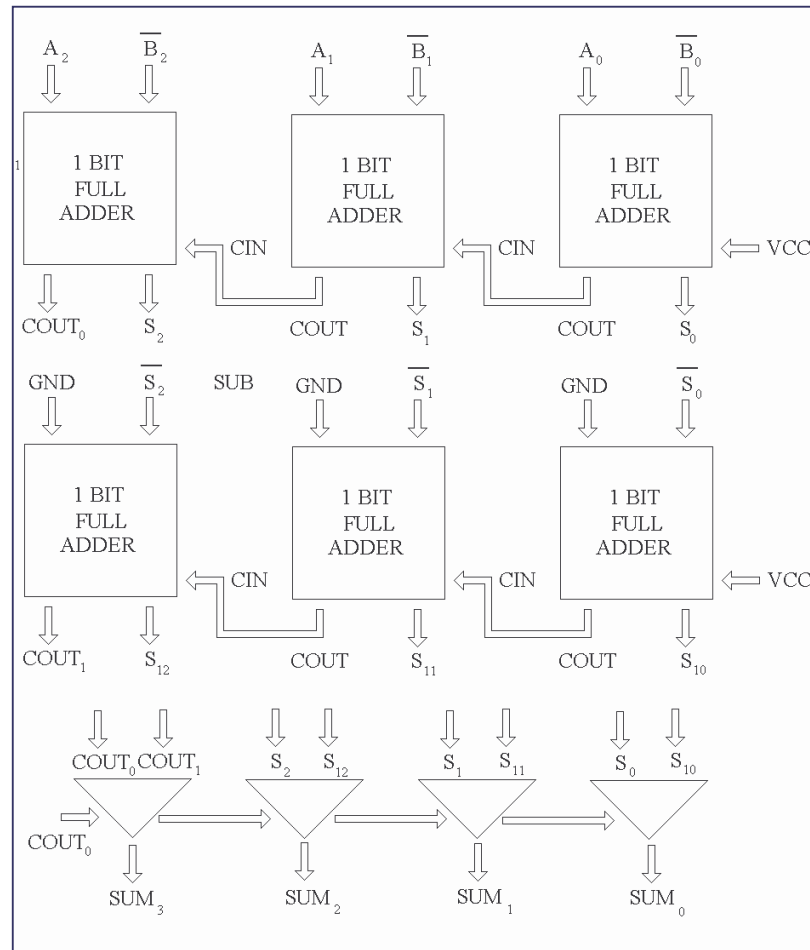


Figure 7: Function A-B Block Diagram

FUNCTION A - B: Modulus Schematics

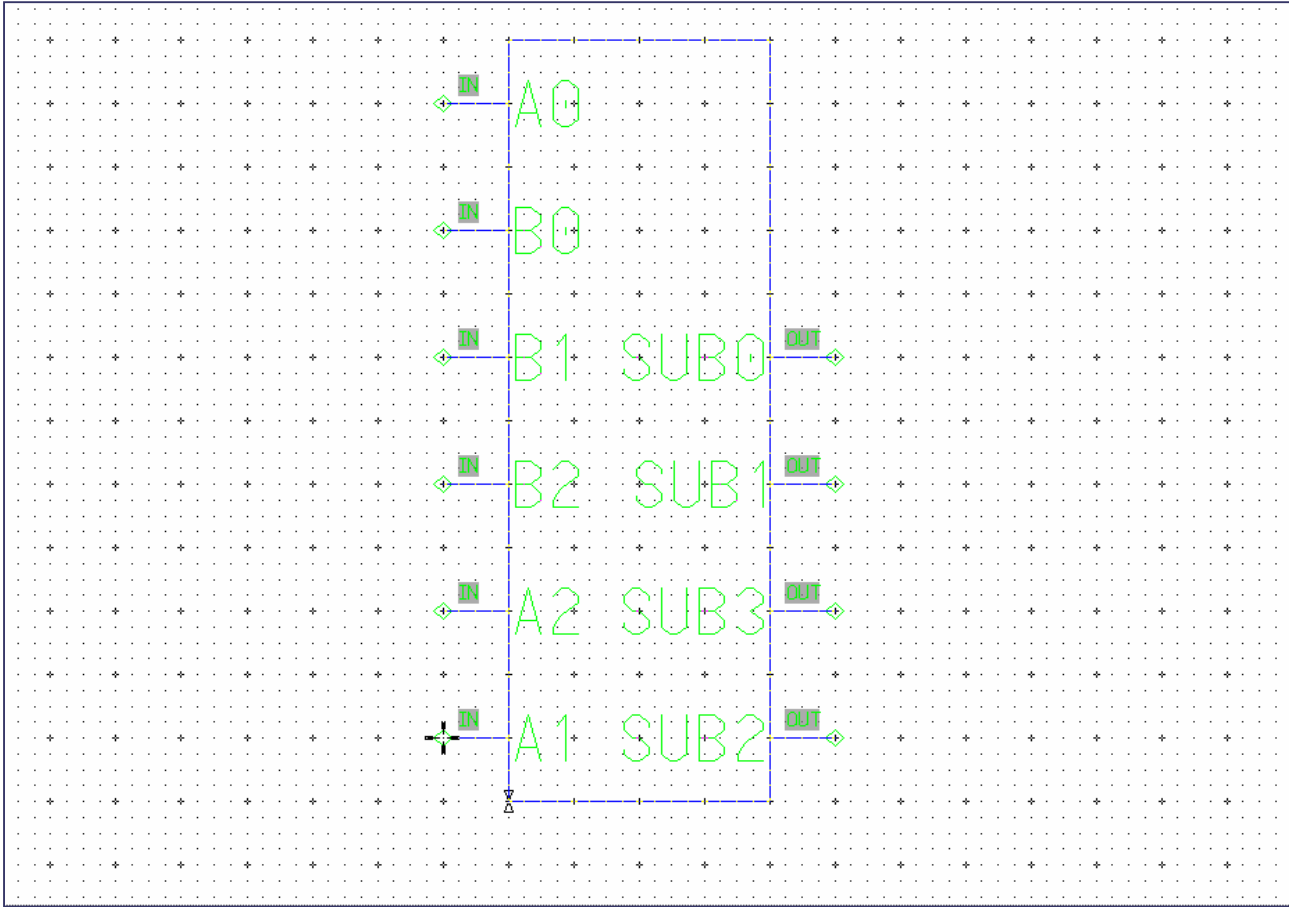


Figure 8: *Function A-B Modulus Schematics*

FUNCTION A - B: Modulus Circuit

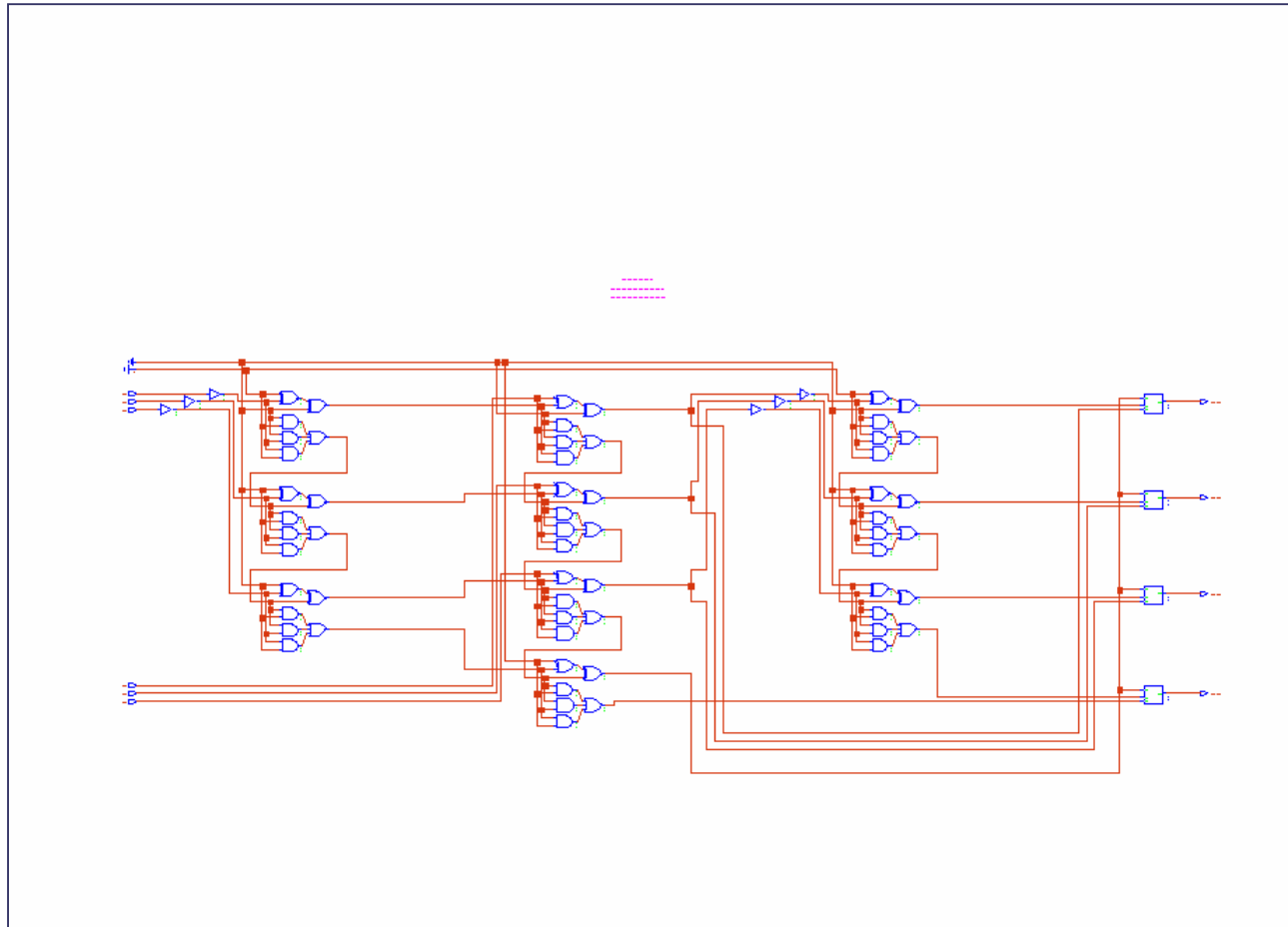


Figure 9: Function A-B Modulus Circuit

FUNCTION $A \oplus B$: Block Diagram

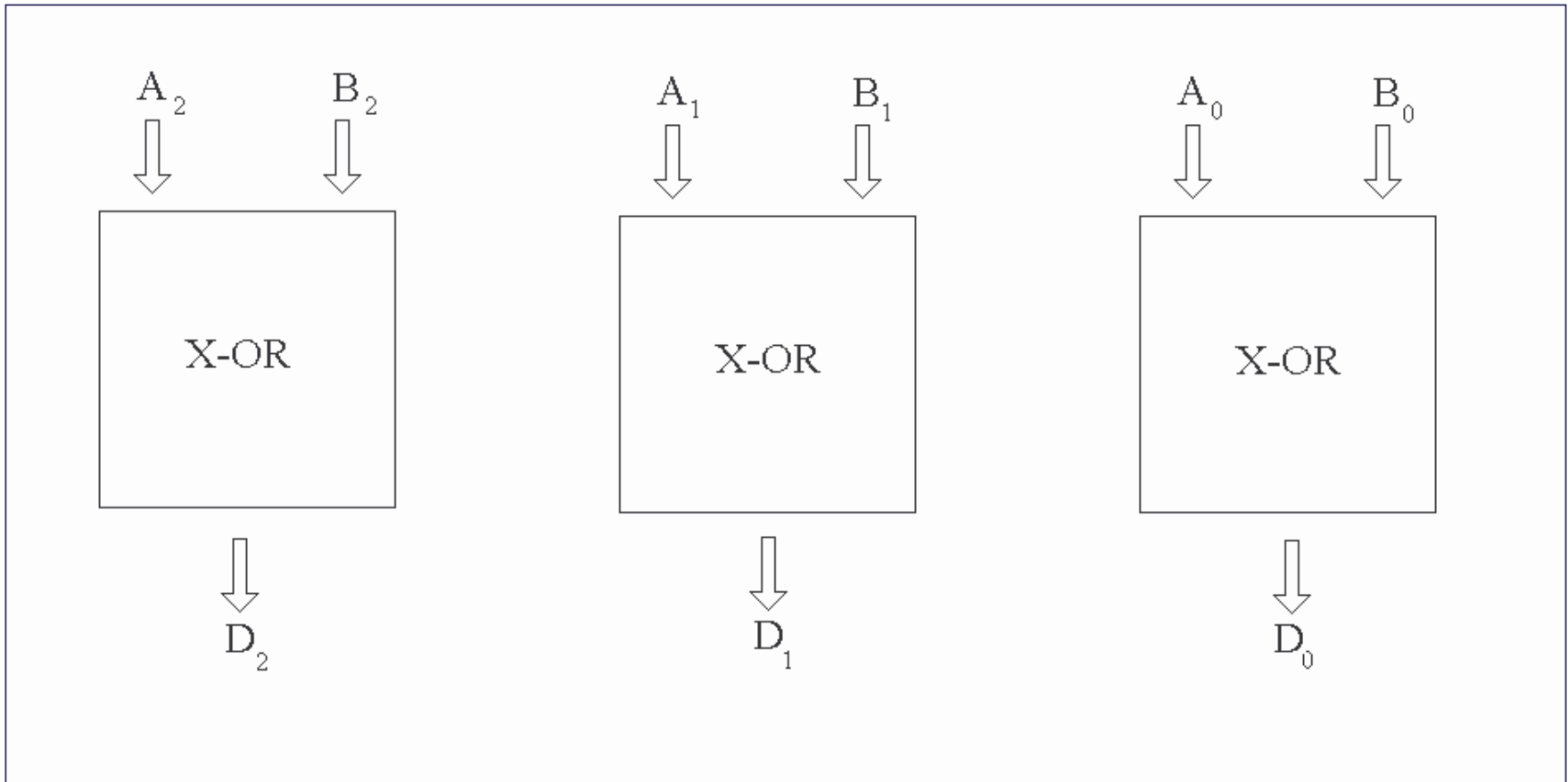


Figure 10: *Function $A \oplus B$ Block Diagram*

FUNCTION $A \oplus B$: Modulus Schematics

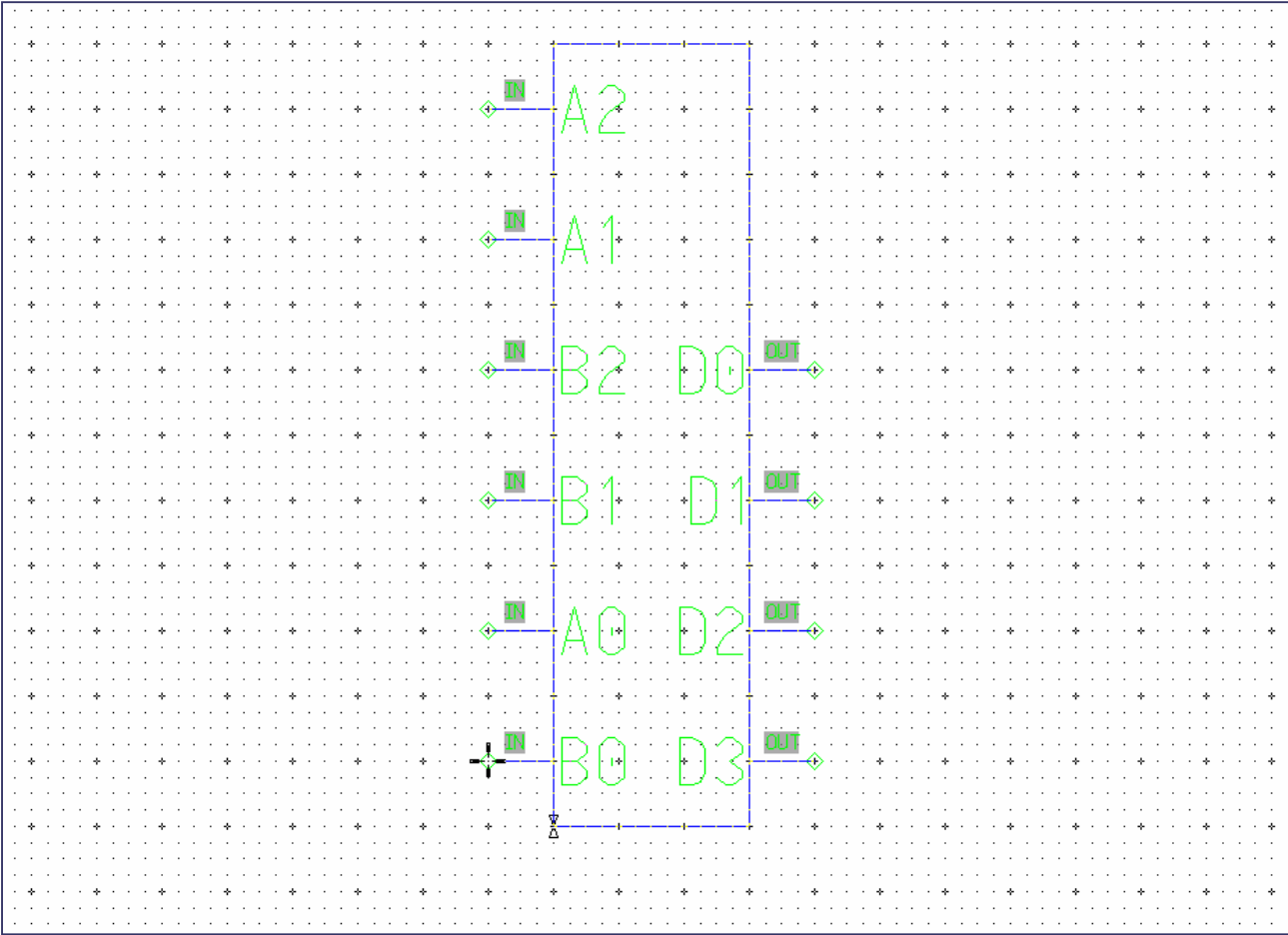


Figure 11: *Function $A \oplus B$ Modulus Schematics*

FUNCTION $A \oplus B$: Modulus Circuit

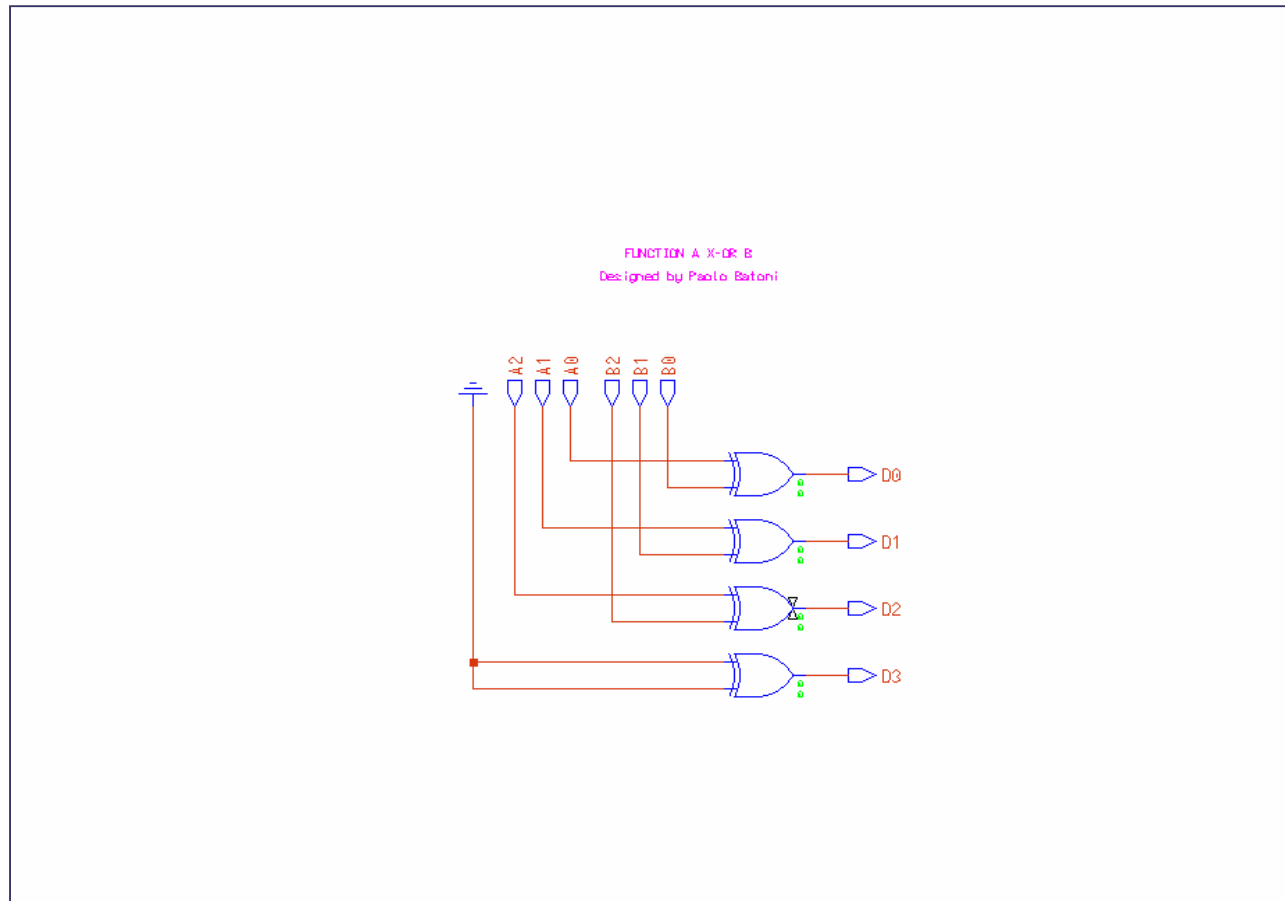


Figure 12: Function $A \oplus B$ Modulus Circuit

FUNCTION A': Block Diagram

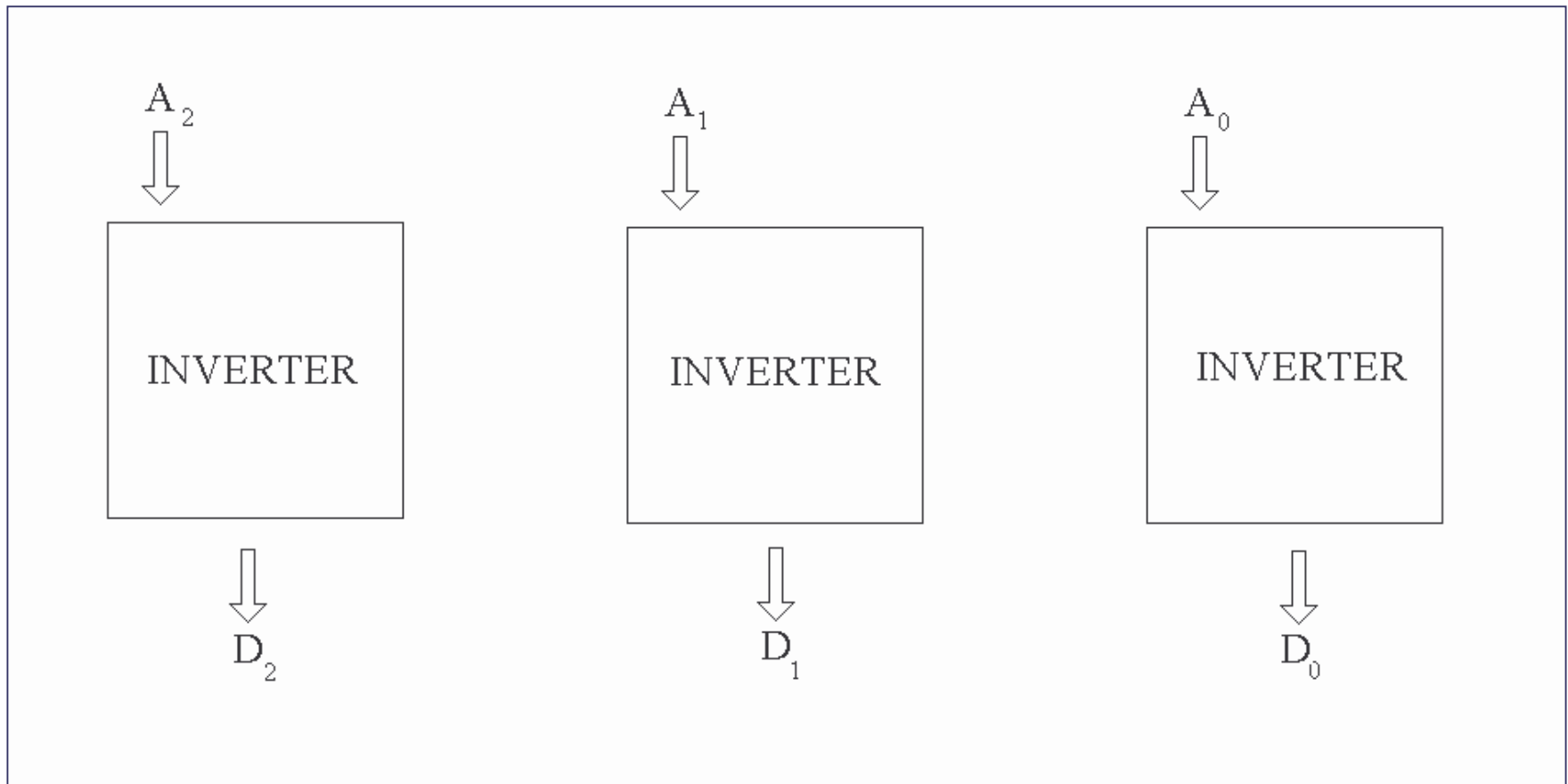


Figure 13: *Function A' Block Diagram*

FUNCTION A': Modulus Schematics

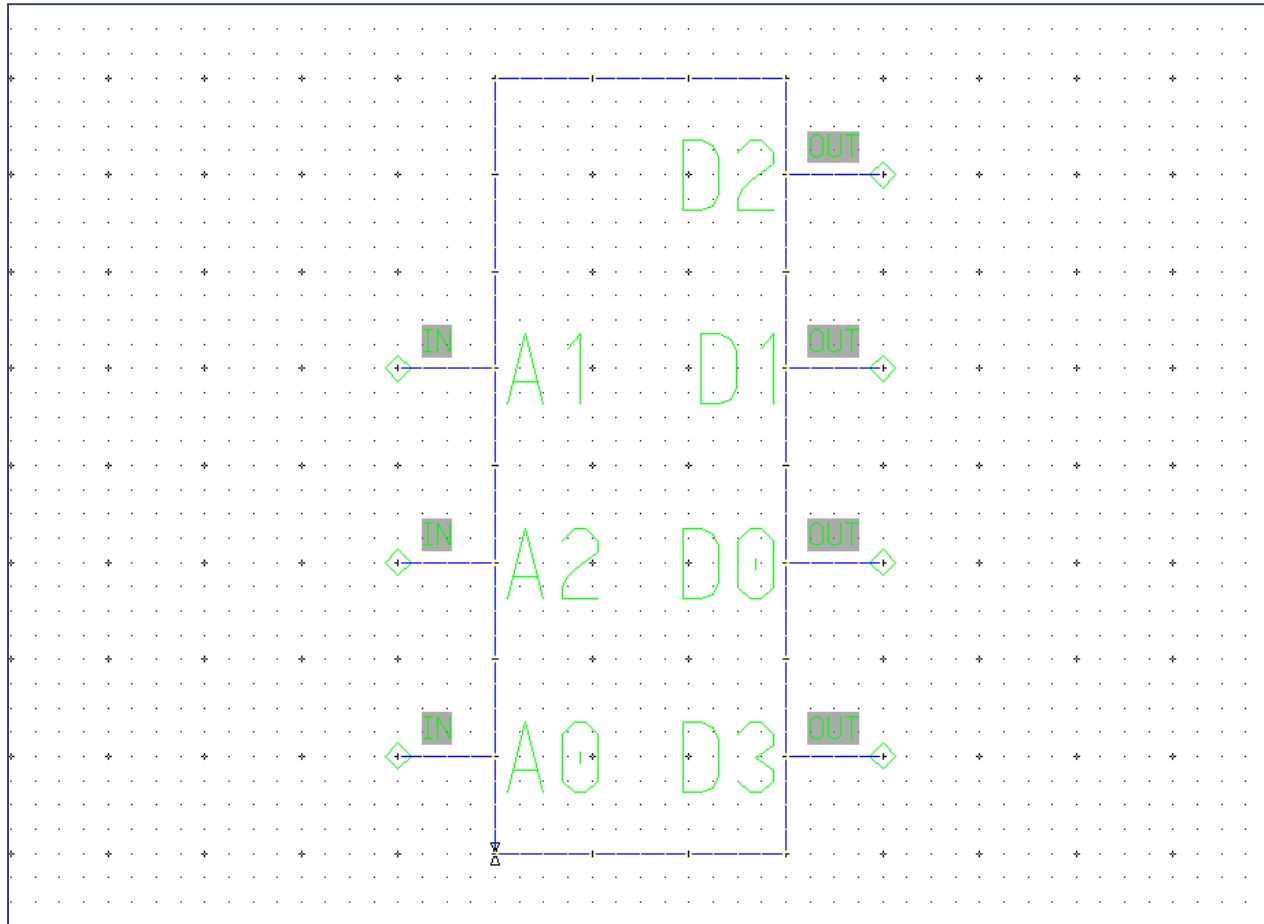


Figure 14: Function A' Modulus Schematics

FUNCTION A': Modulus Circuit

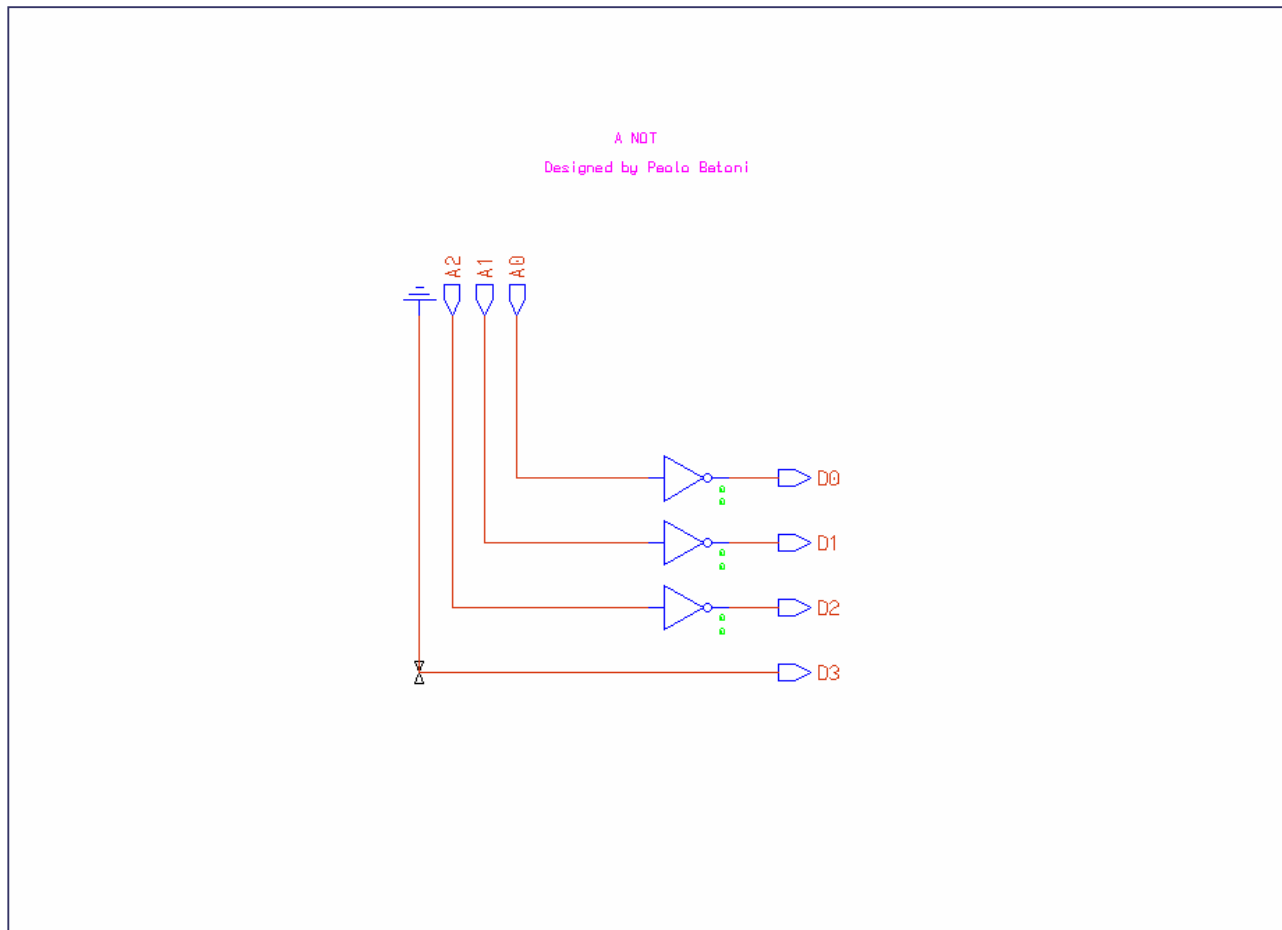


Figure 15: Function A' Modulus Circuit

FUNCTION B': Block Diagram

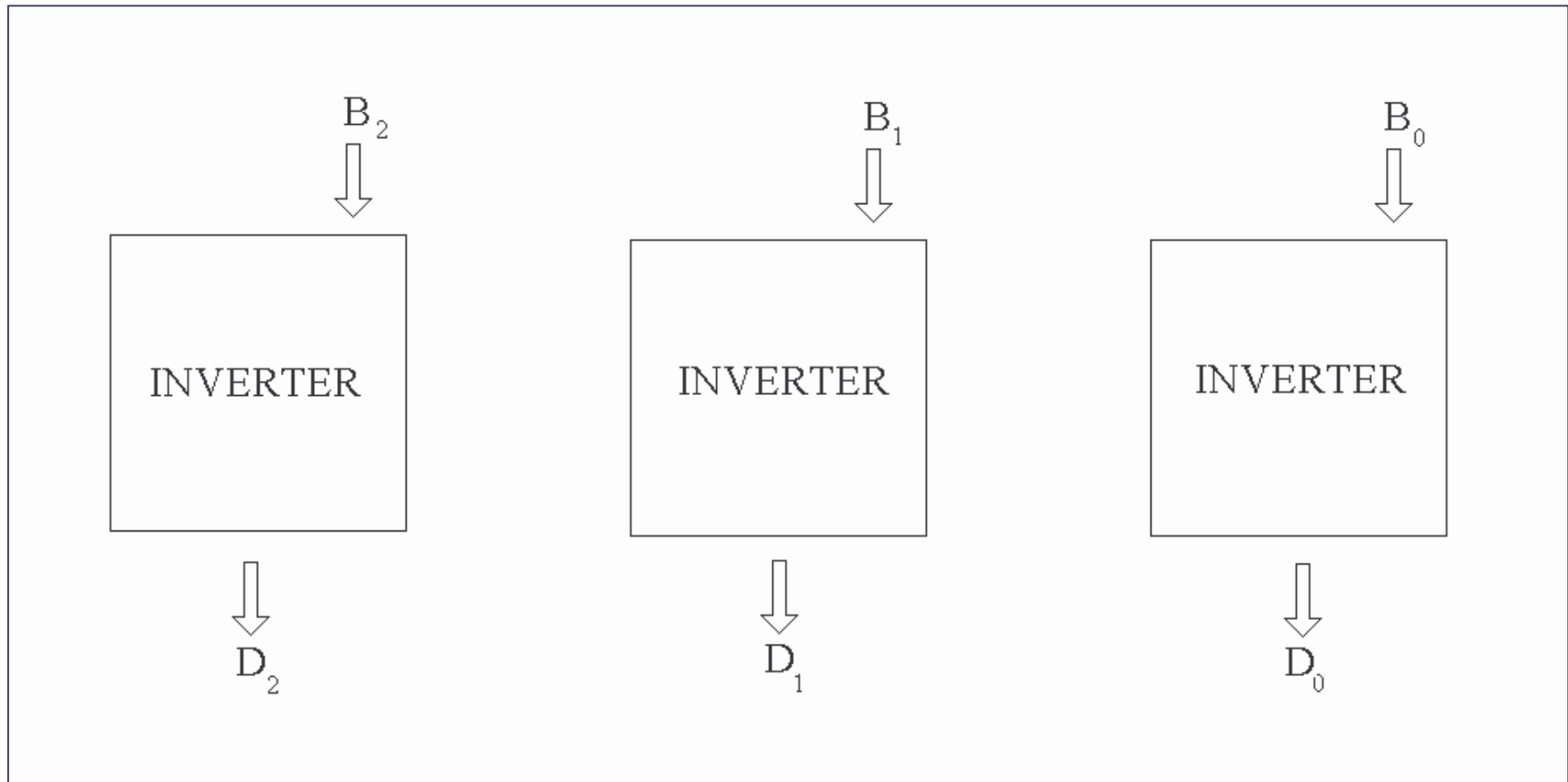


Figure 16: *Function B' Block Diagram*

FUNCTION B': Modulus Schematics

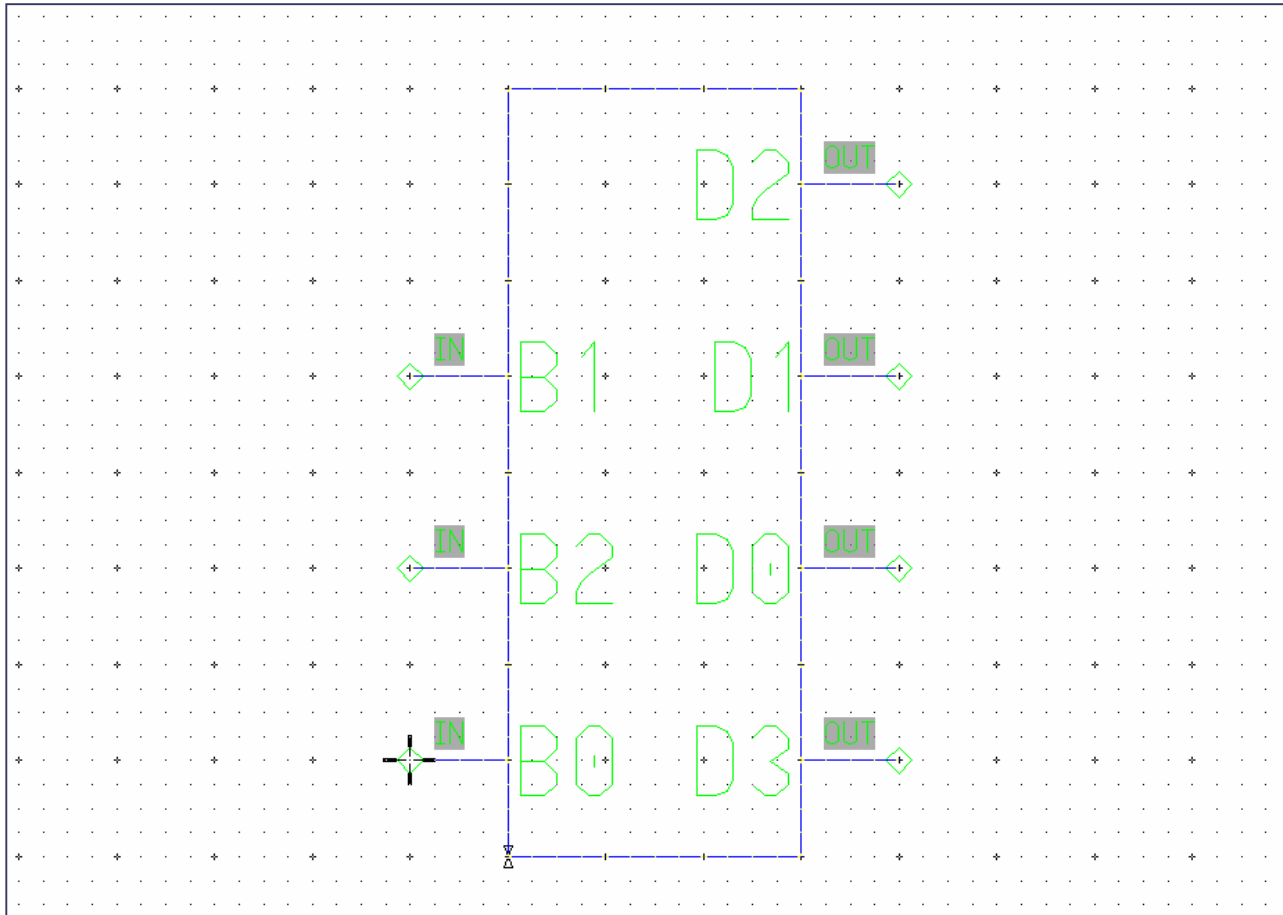


Figure 17: Function B' Modulus Schematics

FUNCTION B': Modulus Circuit

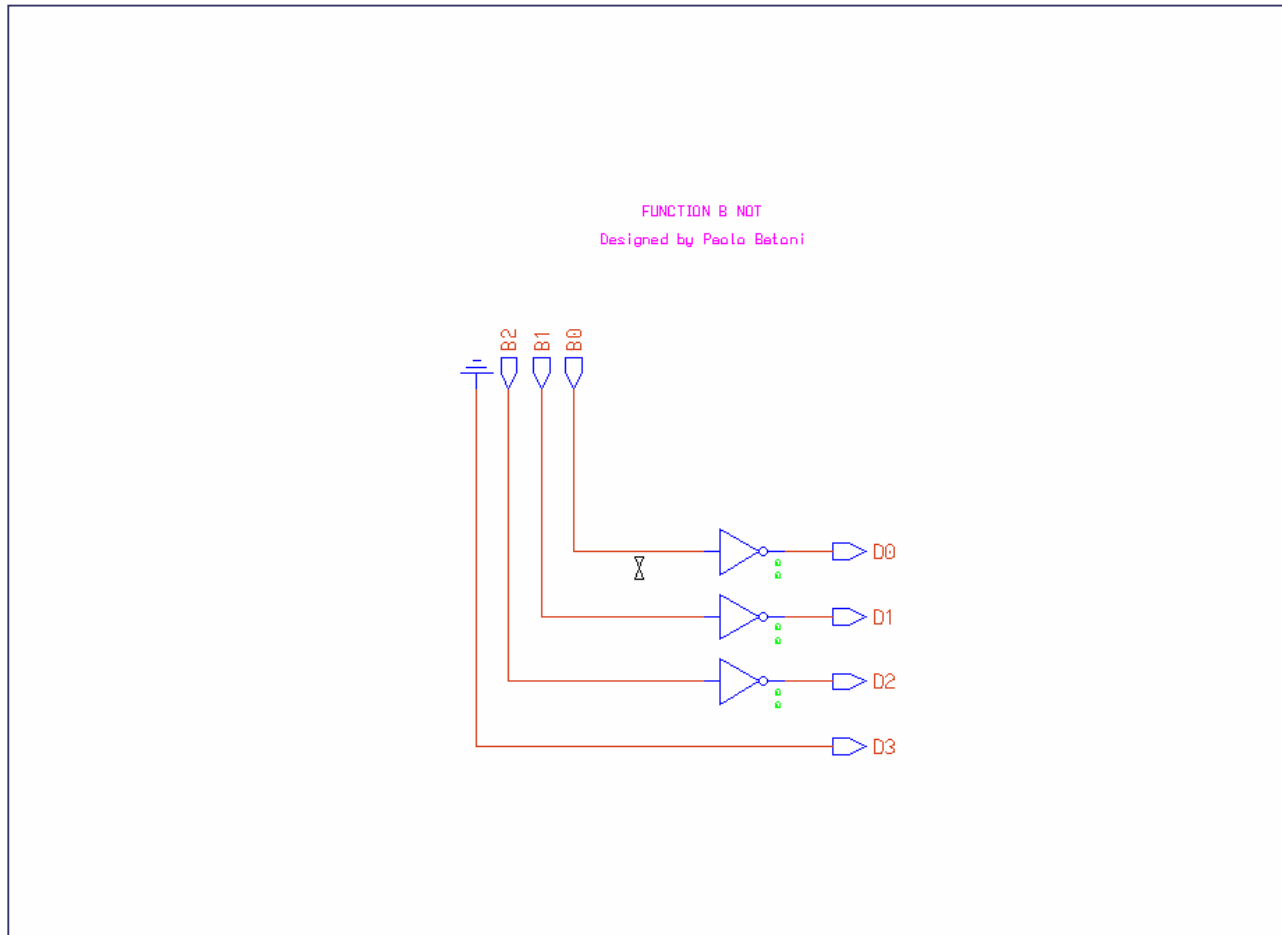


Figure 18: Function B' Modulus Circuit

FUNCTION 0001: Modulus Schematics

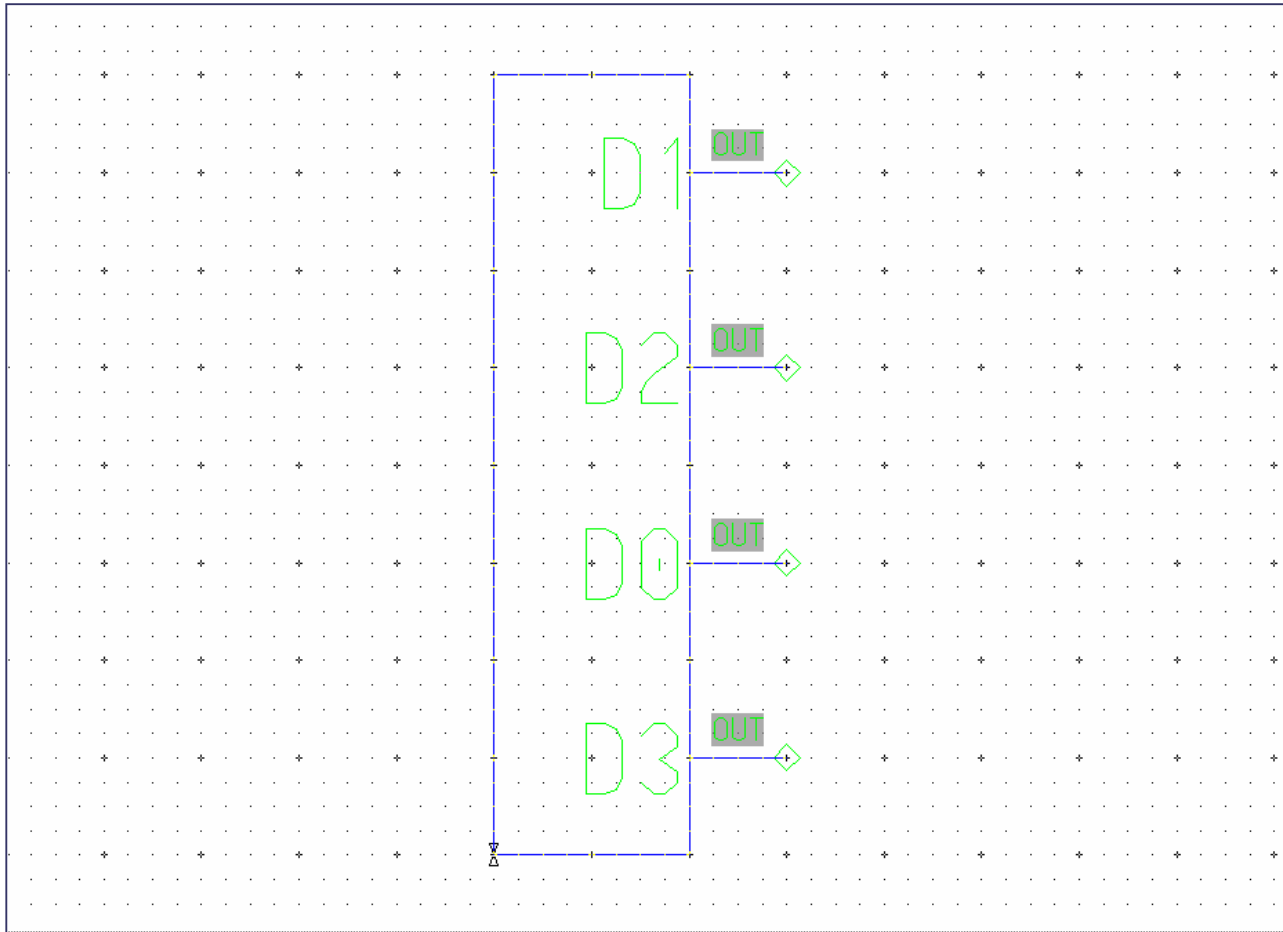


Figure 19: Function 0001 Modulus Schematics

FUNCTION 0001: Modulus Circuit

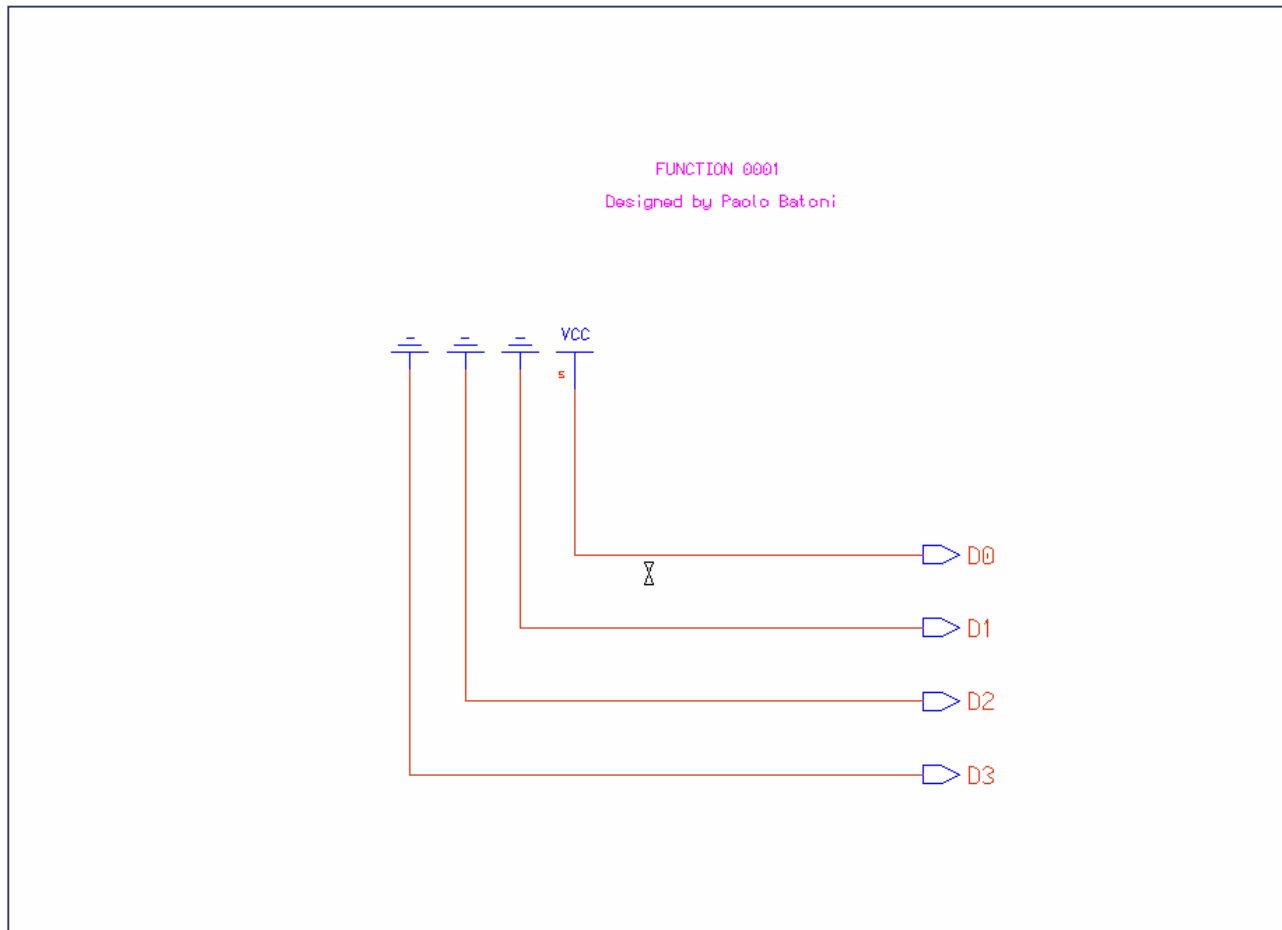


Figure 20: *Function 0001 Modulus Circuit*

FUNCTION 2'S of A: Block Diagram

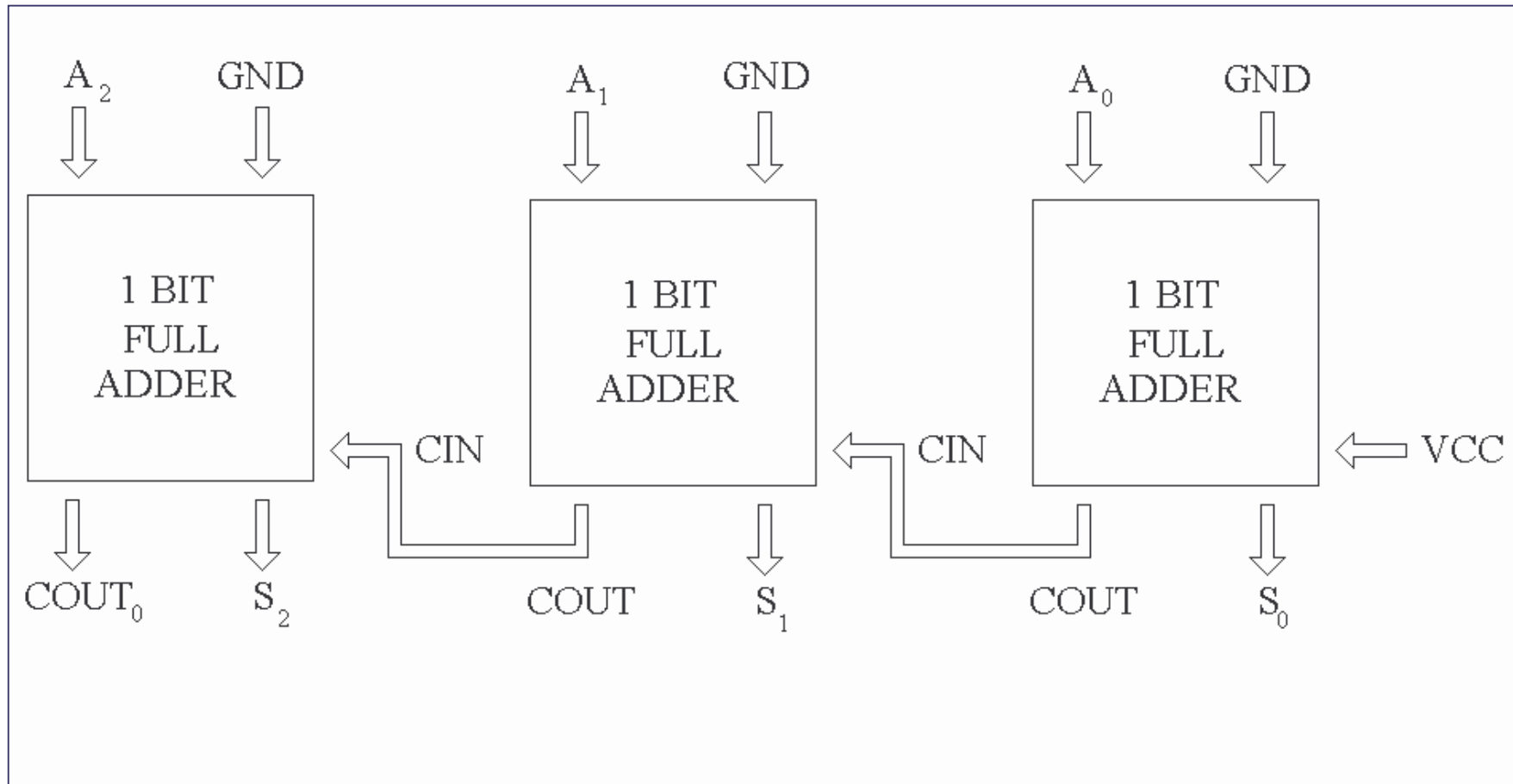


Figure 21: 2'S Complement of A Block Diagram

FUNCTION 2'S of A: Modulus Schematics

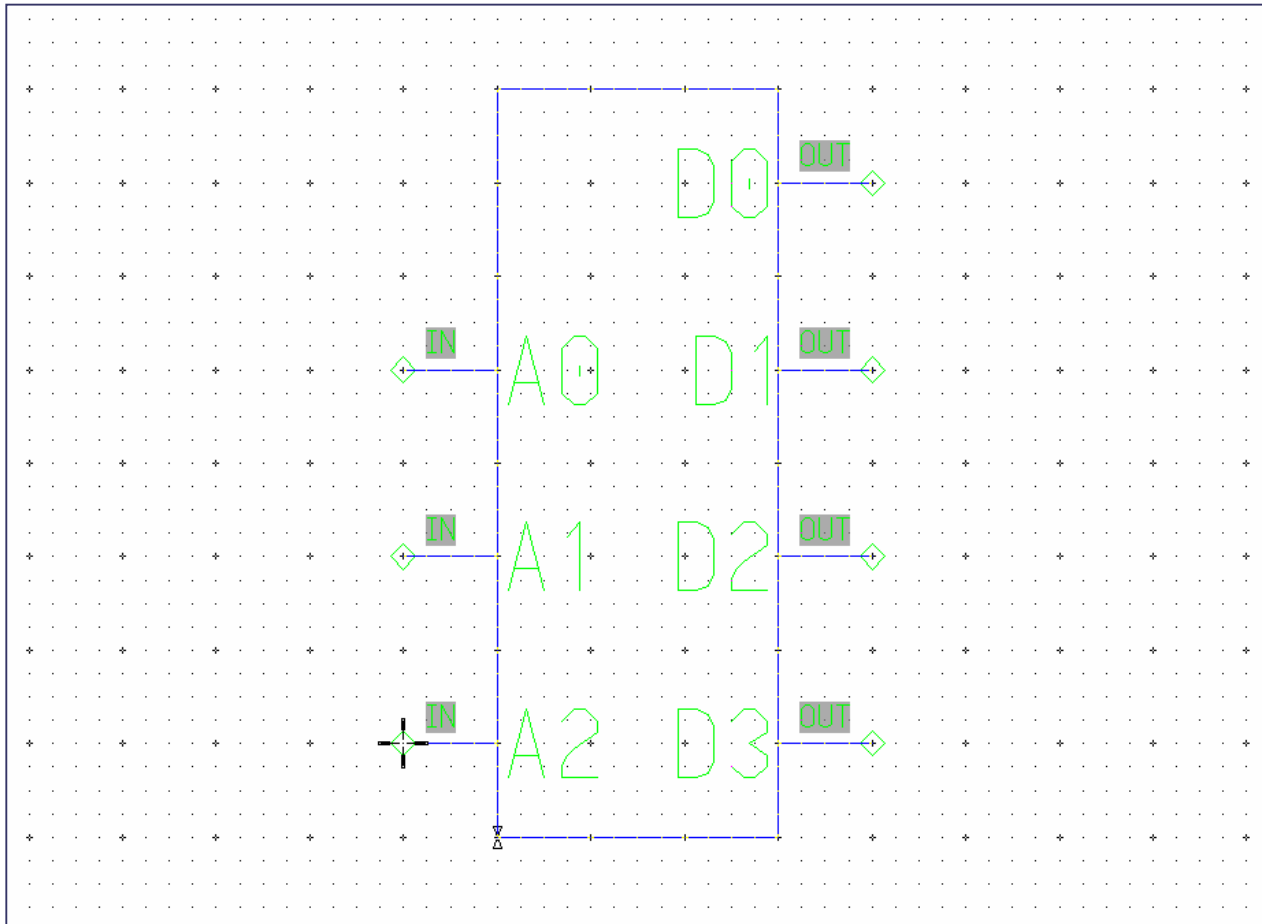


Figure 22: Function 2'S of A Modulus Schematics

FUNCTION 2'S of A: Modulus Circuit

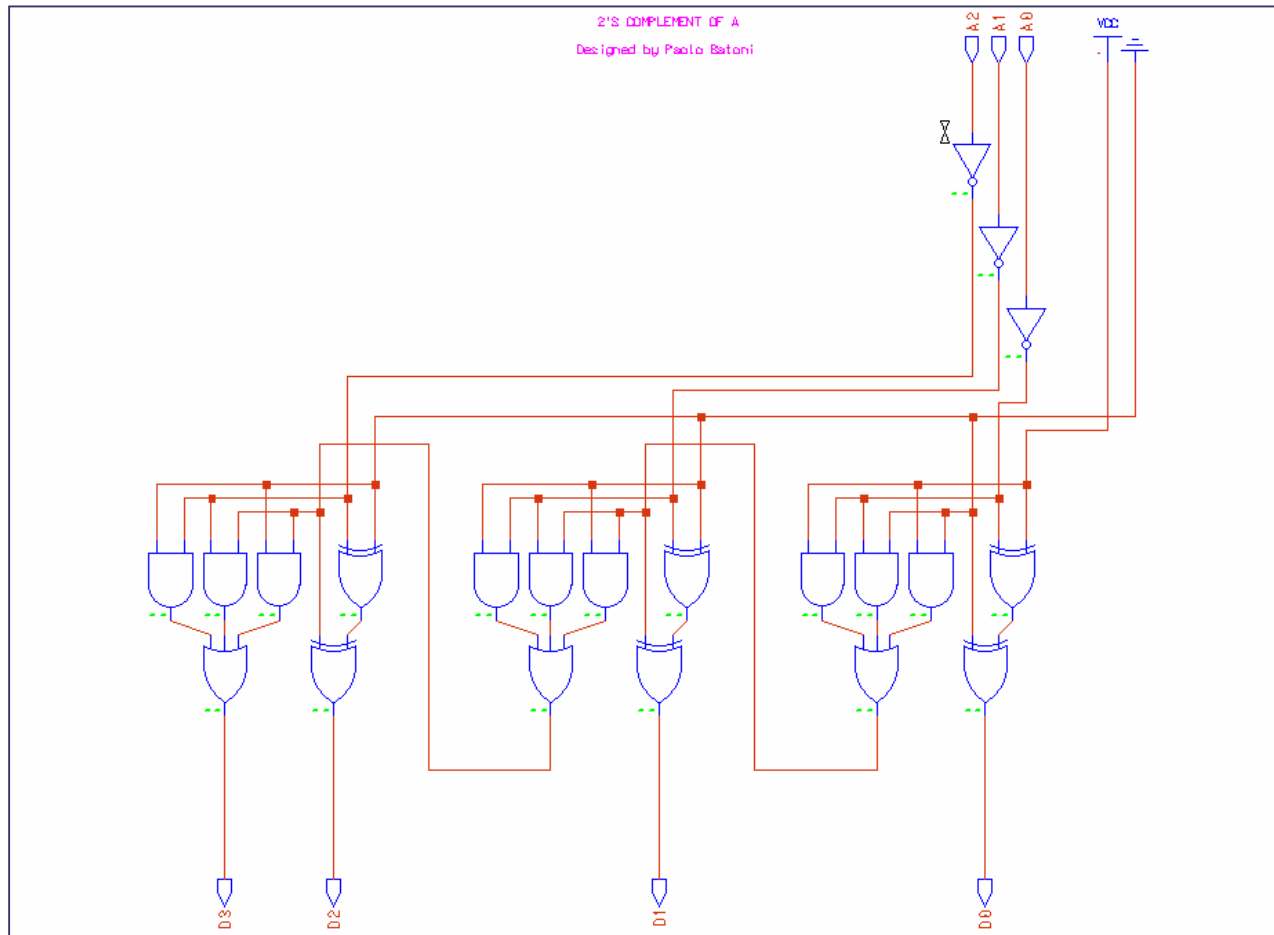


Figure 23: 2'S of A Modulus Circuit

FUNCTION A NAND B: Block Diagram

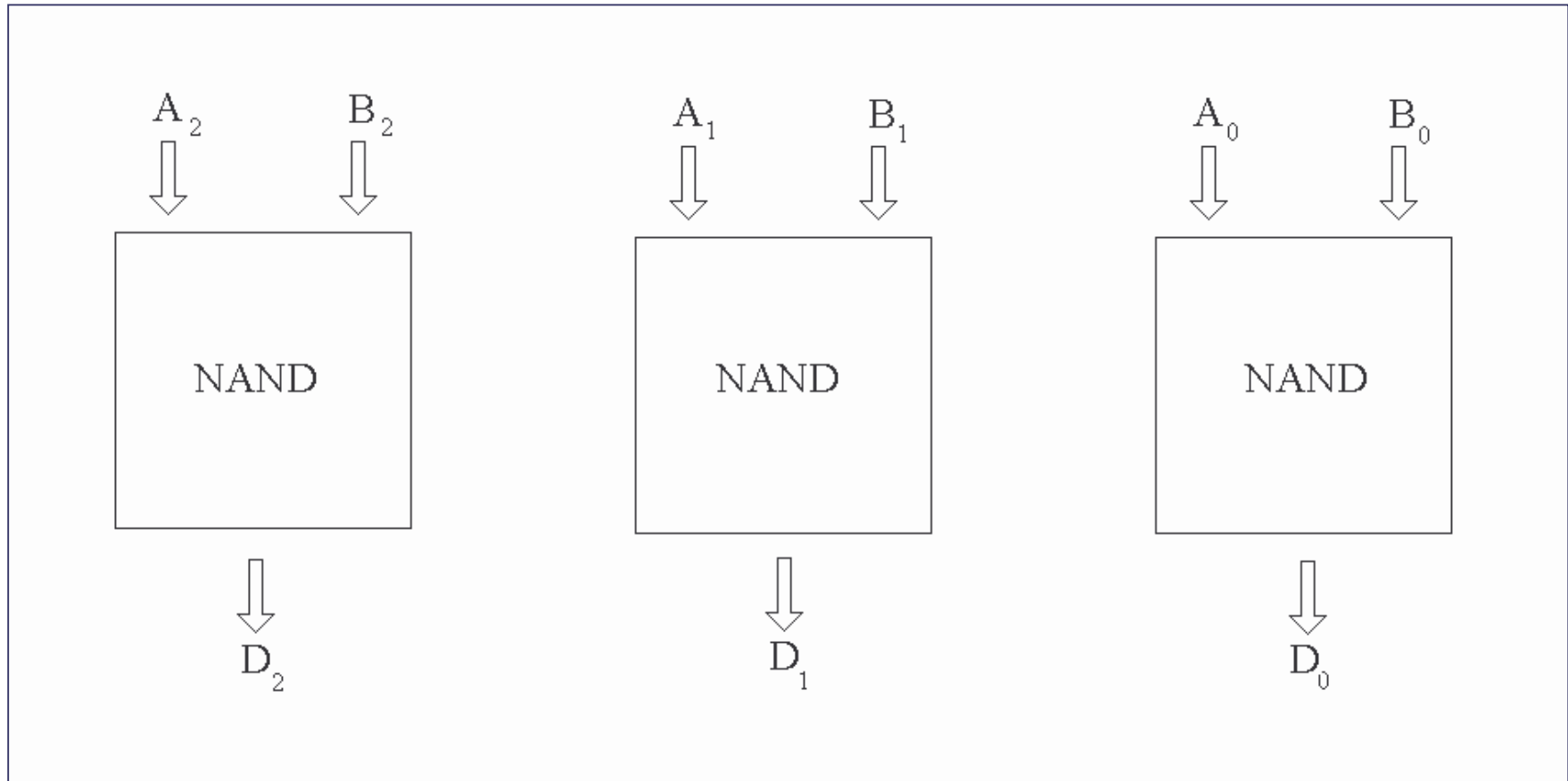


Figure 24: Function A NAND B Block Diagram

FUNCTION A NAND B: Modulus Schematics

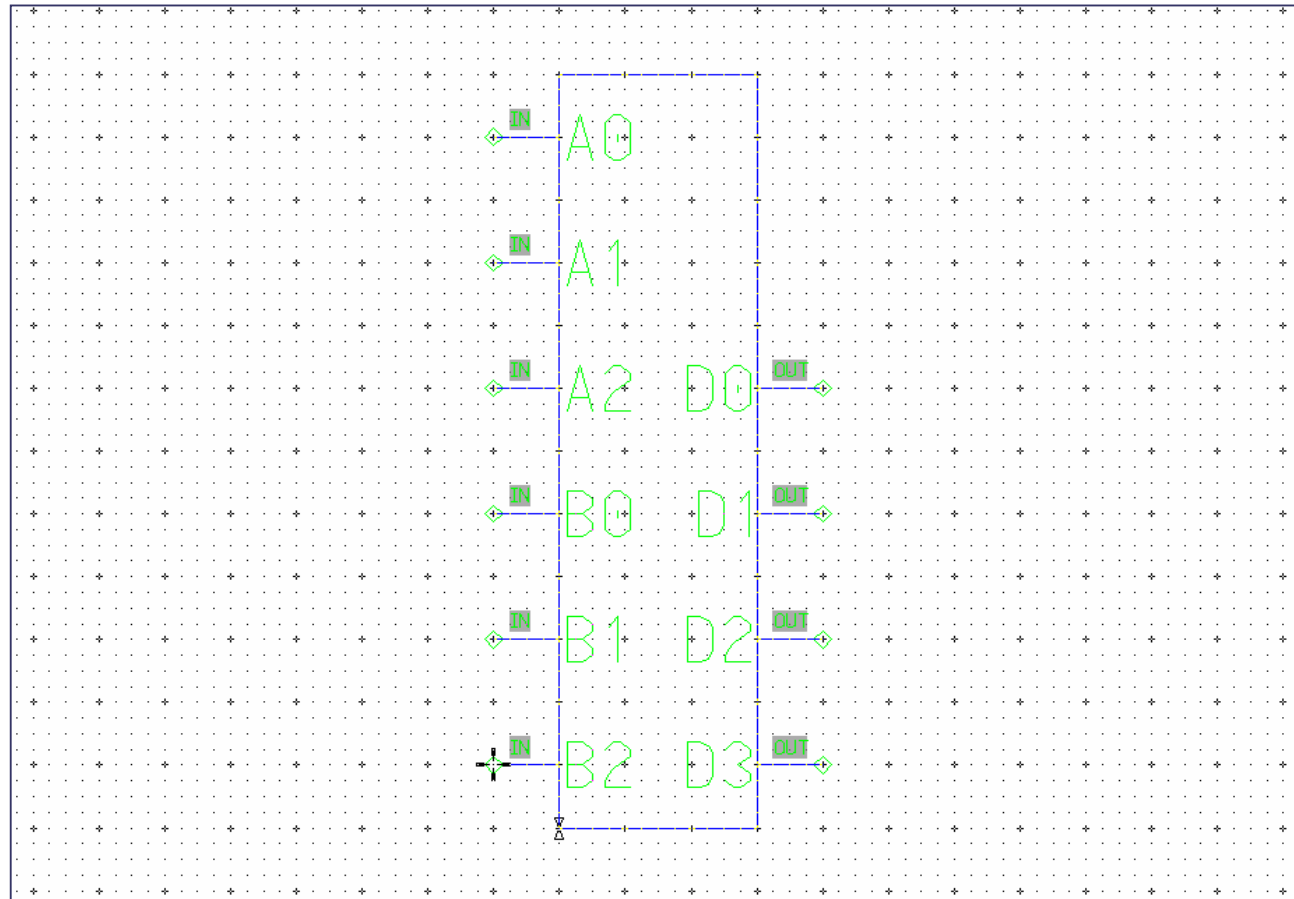


Figure 25: Function A NAND B Modulus Schematics

FUNCTION A NAND B: Modulus Circuit

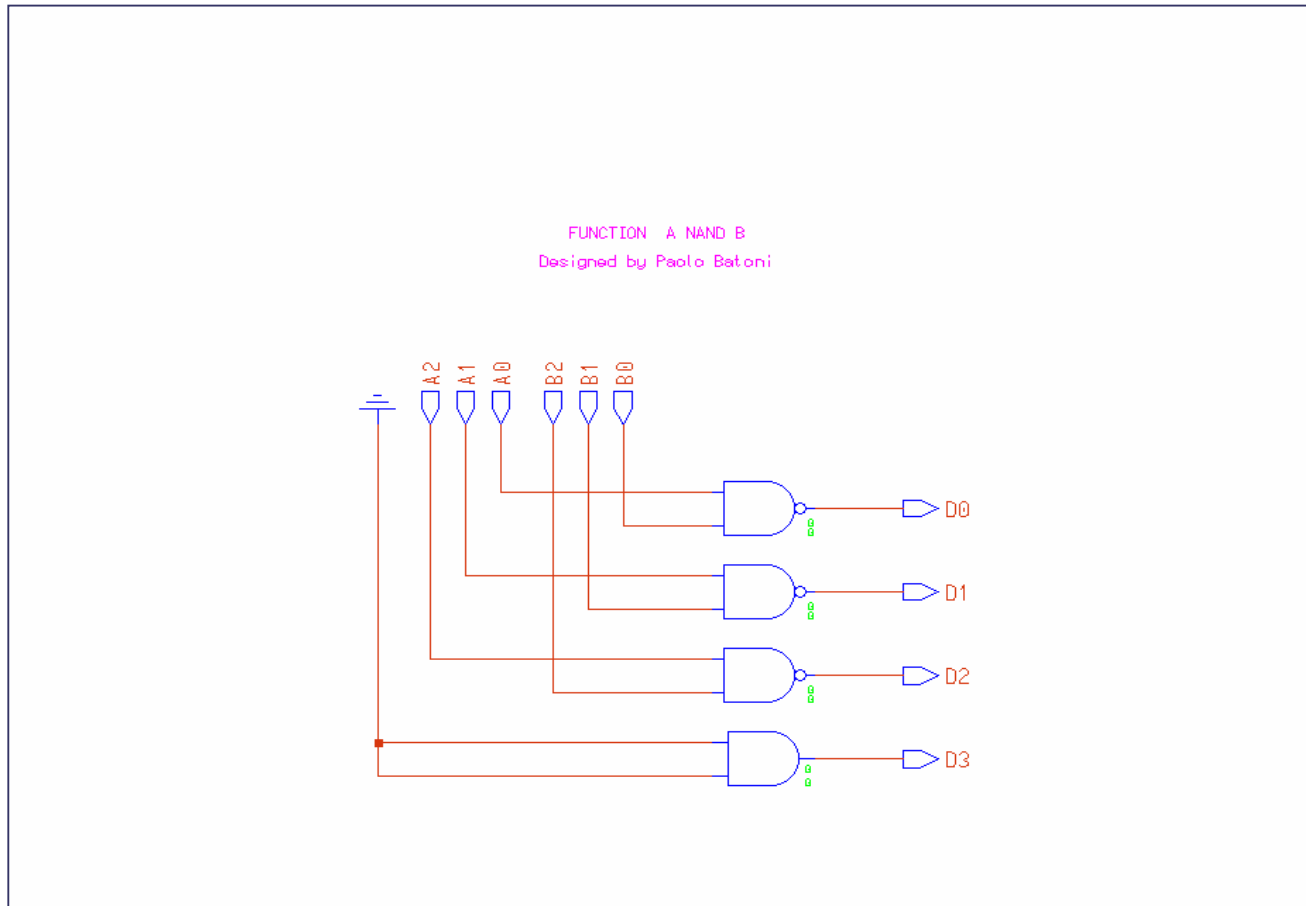


Figure 26: *Function A NAND B Modulus Circuit*

FUNCTION G: Modulus Schematics

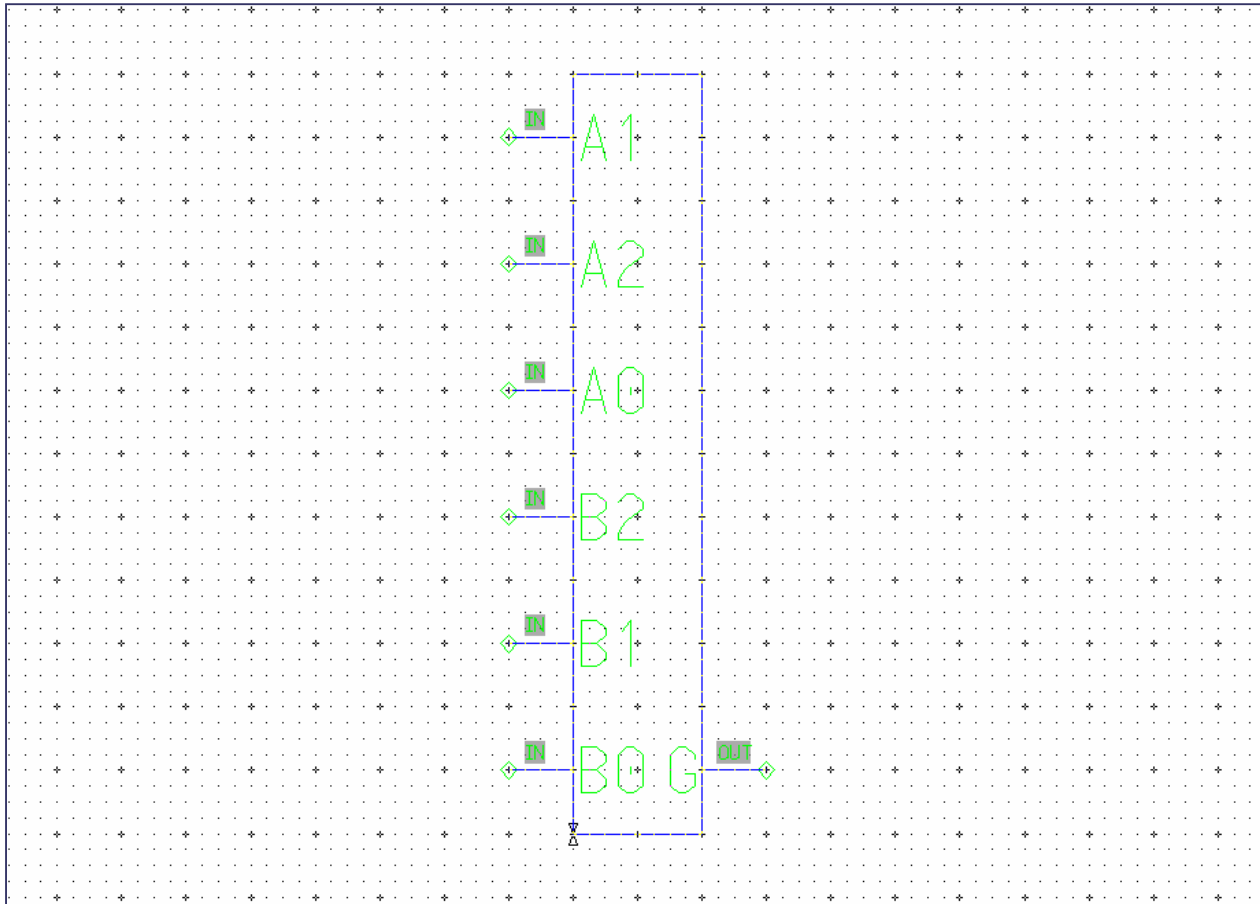


Figure 27: Function G Modulus Schematics

FUNCTION G: Modulus Circuit

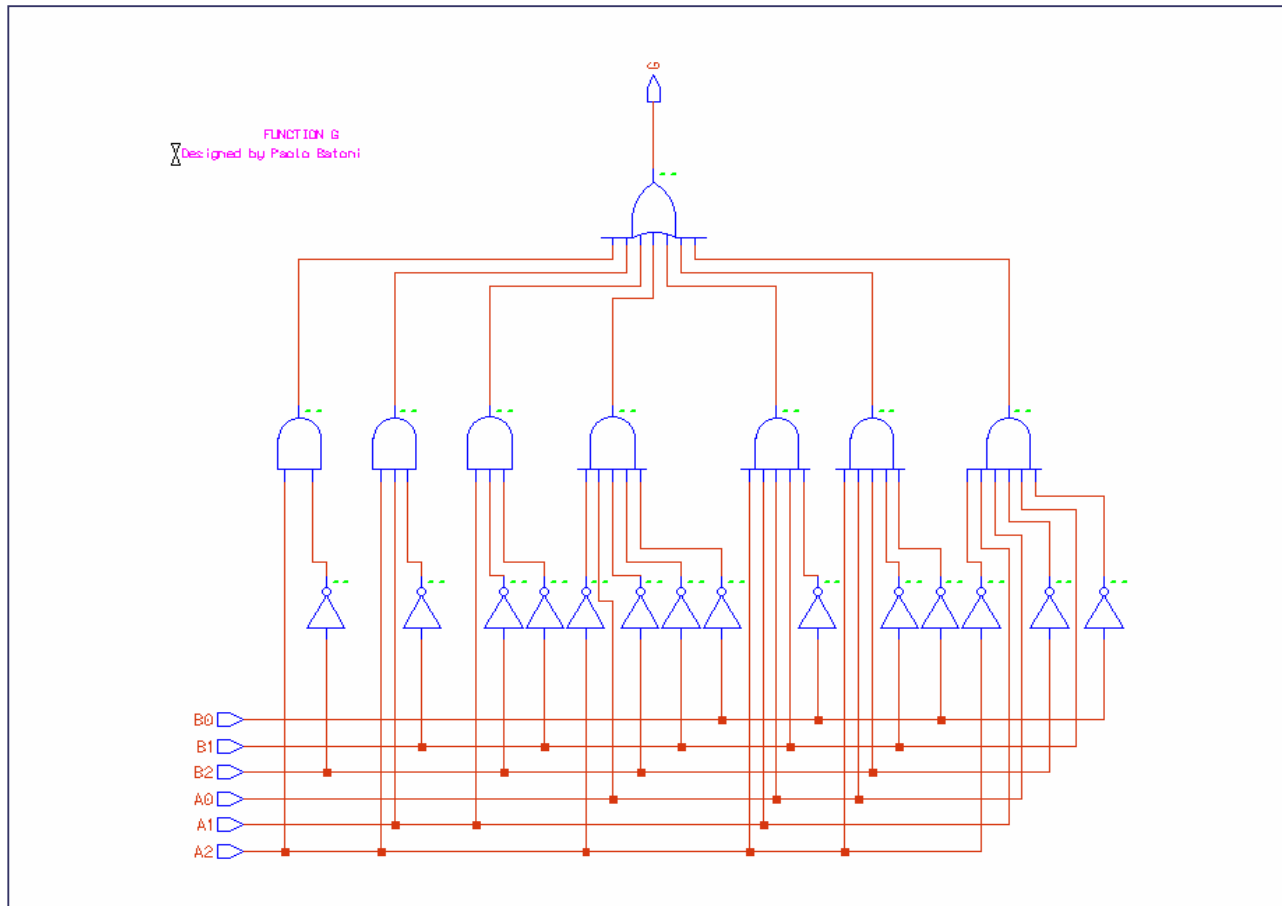


Figure 28: Function G Modulus Circuit

FUNCTION E: Modulus Schematics

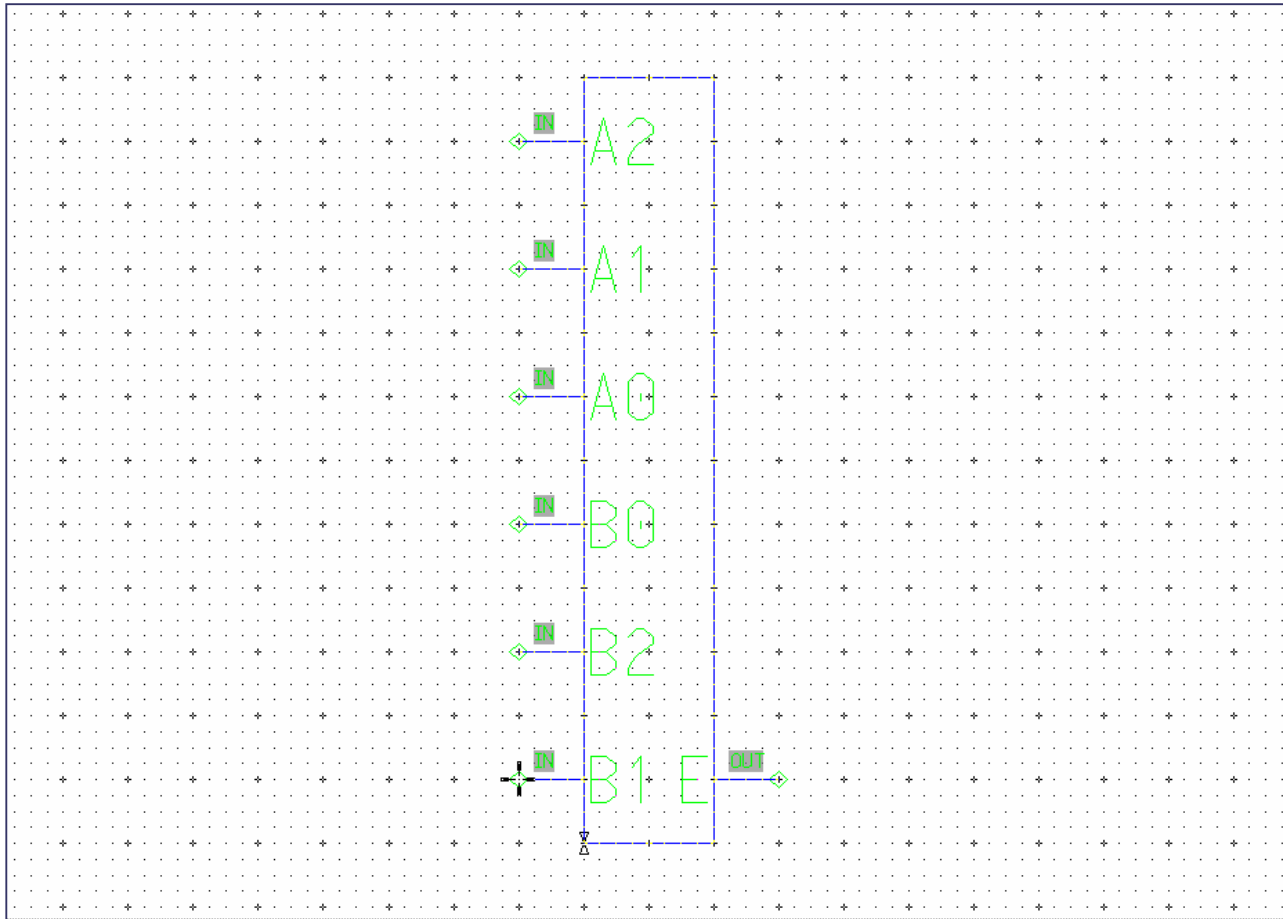


Figure 29: Function E Modulus Schematics

FUNCTION E: Modulus Circuit

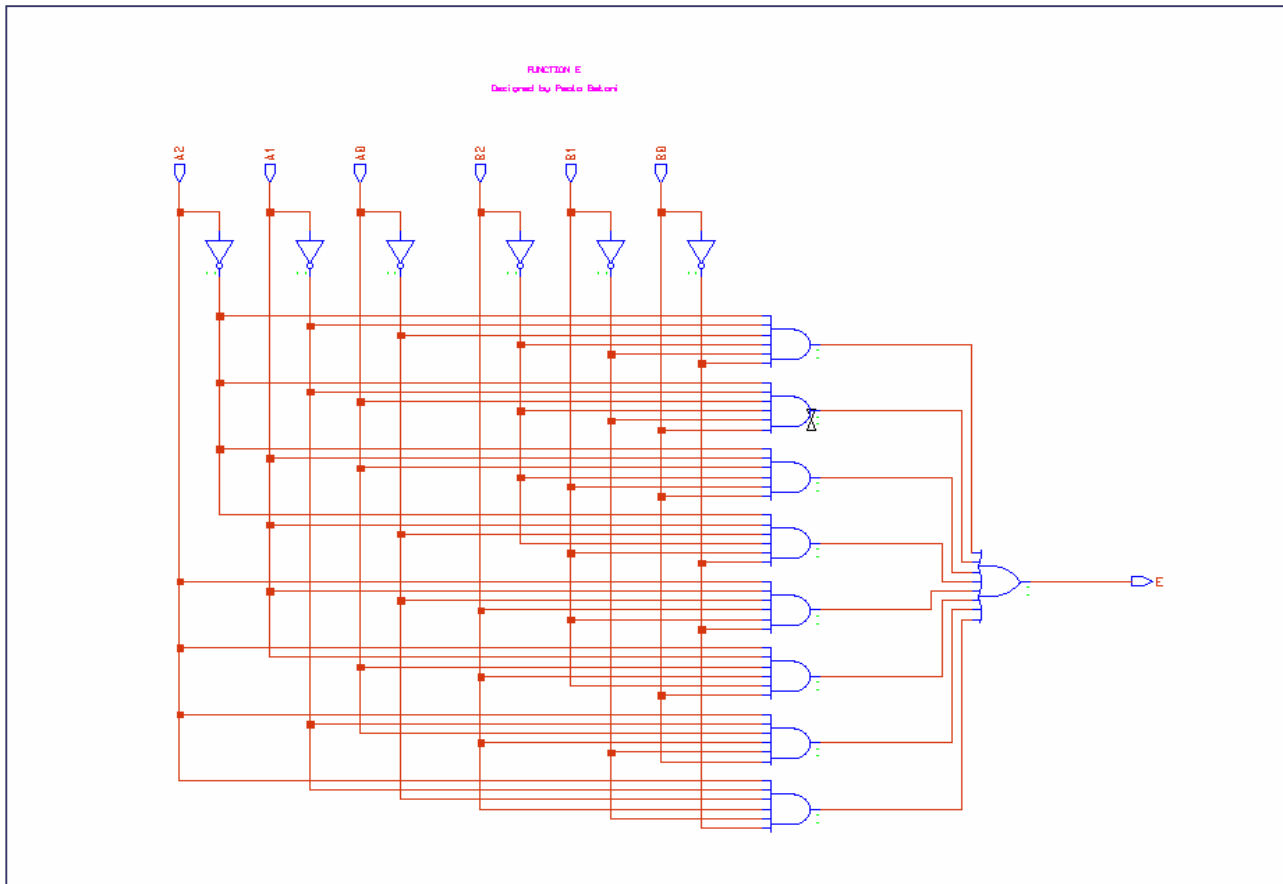


Figure 30: Function E Modulus Circuit

8-TO-1 MULTIPLEXOR: Modulus Schematics

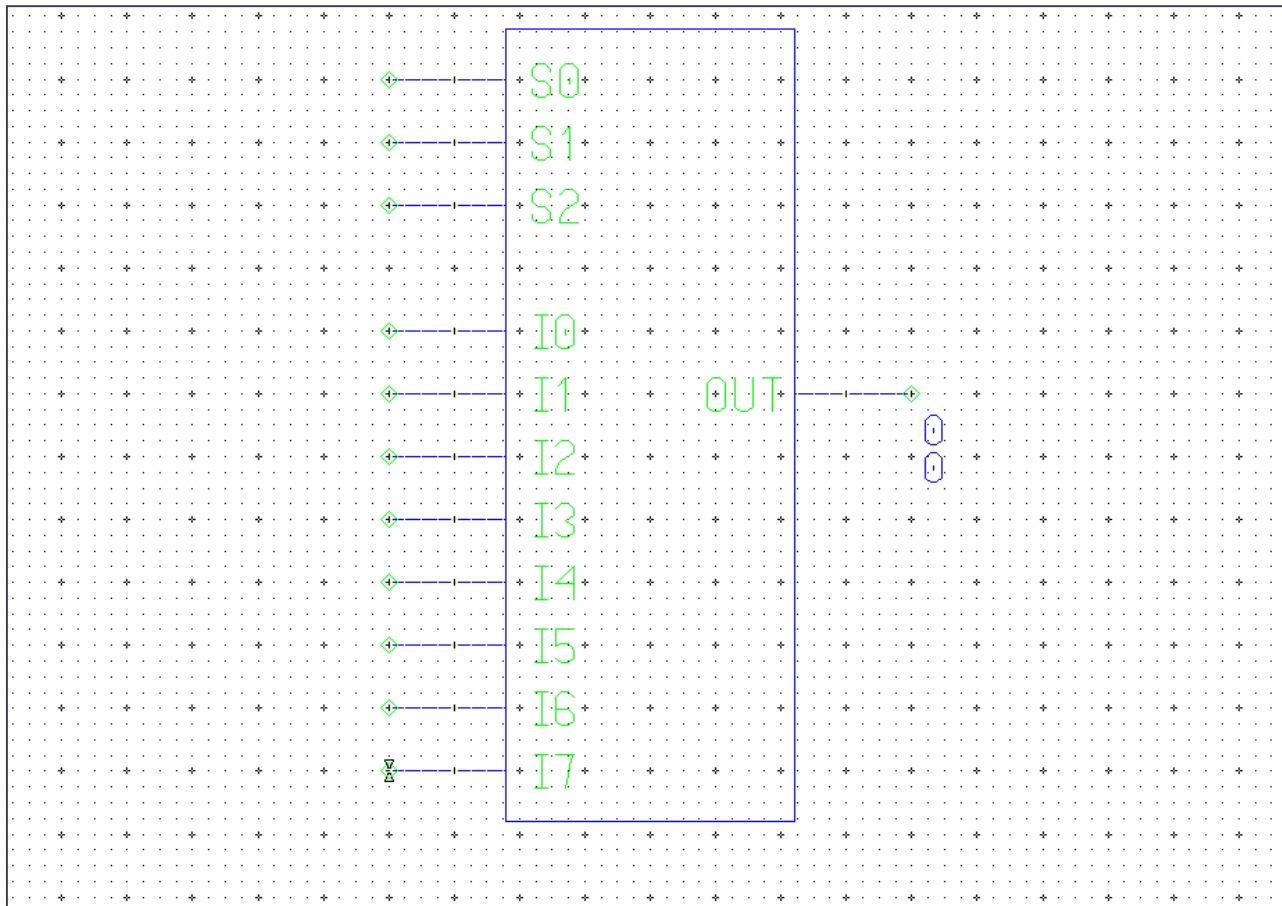


Figure 31: 8-TO-1 Multiplexor Modulus Schematics

8-TO-1 MULTIPLEXOR: Modulus Circuit

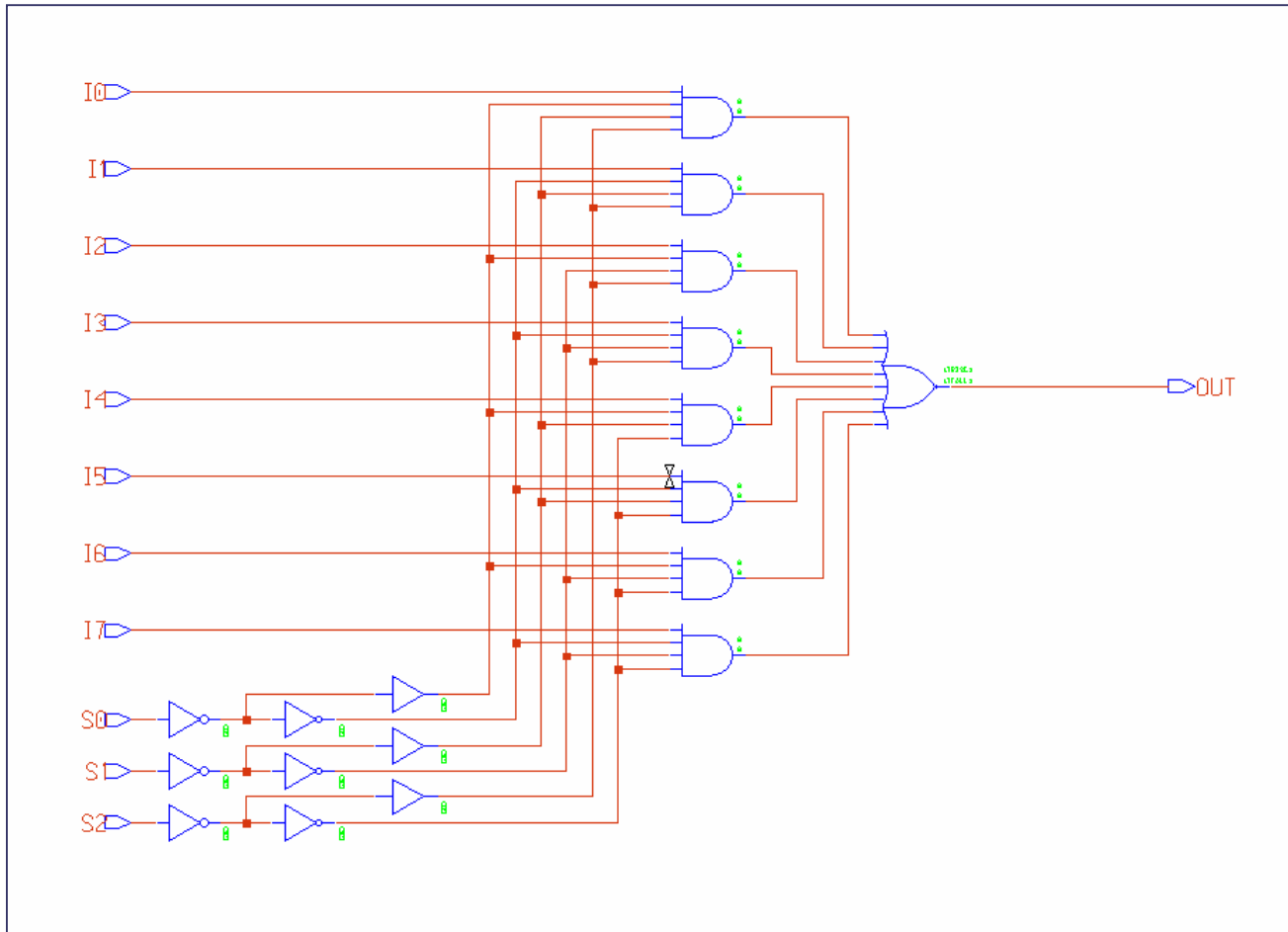


Figure 32: 8-TO-1 Multiplexor Modulus Circuit

SIMULATION STRATEGY

In order to conduct a time-efficient simulation of the “2181” ALU Project, and in order to guarantee a 100% error proof, each single module of the entire logic circuit implemented, simulated, and tested with Mentor Graphics running on a Sun Spark Station 5.

The simulation of each of the logic modules was conducted by varying their relative input, which was controlled by a clock function offered by Mentor Graphics itself. While keeping the duty cycle of the input signal constant, the period of the input signal was progressively doubled in order to cover all of the possible input signal combinations. Such a simulating method guaranteed a very rapid and global reading of the output of each of the logic modules.

The “2181” ALU Project was then assembled by connecting all of the logic modules through a battery of 8-to-1 MUX’s. The “2181” ALU Project was then simulated and tested by reading its output after varying the MUX controller (Input S.)

"2181" ALU PROJECT: Simulation 1/8

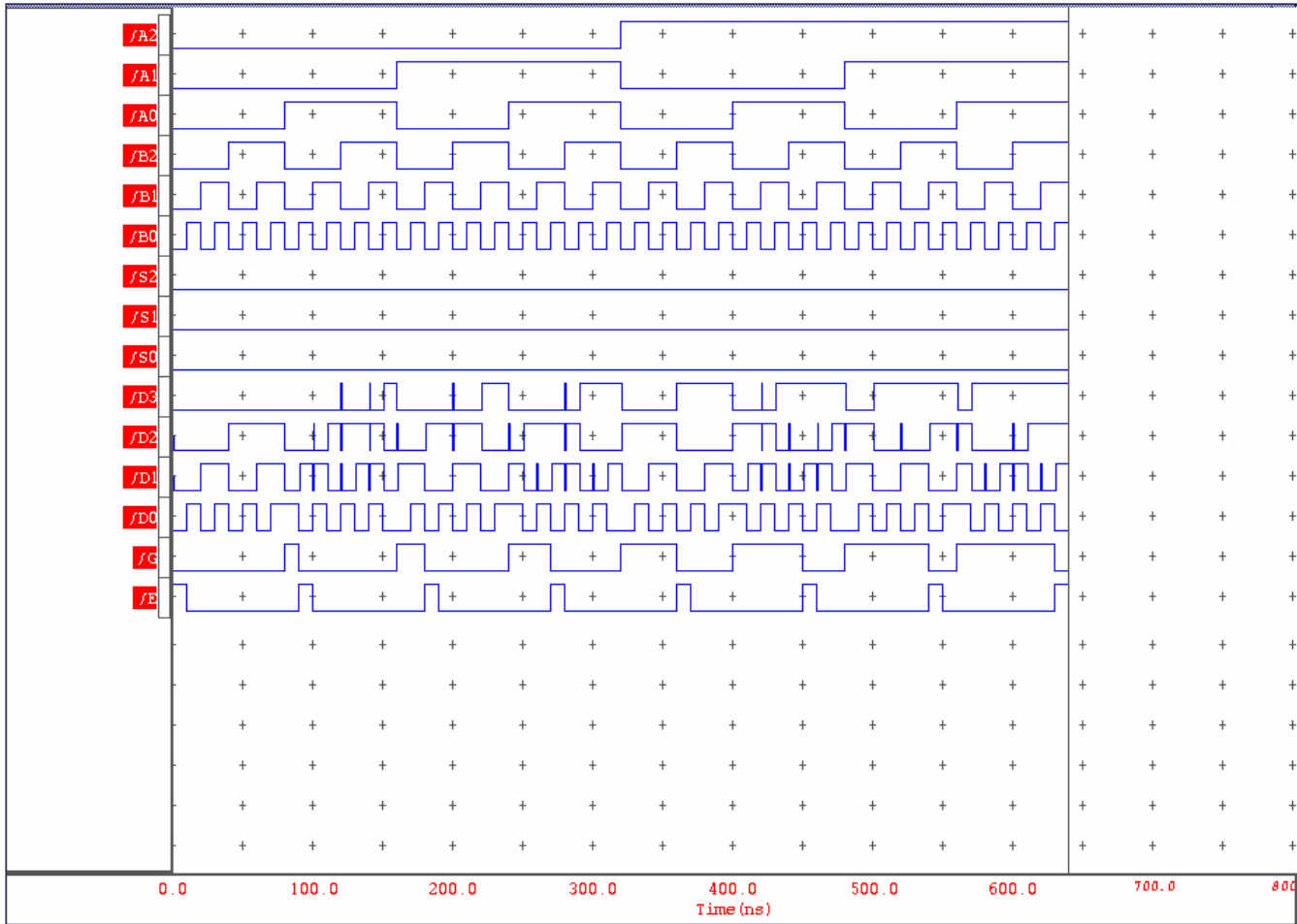


Figure 33: "2181" ALU PROJECT: Simulation 1/8

“2181” ALU PROJECT: Simulation 2/8

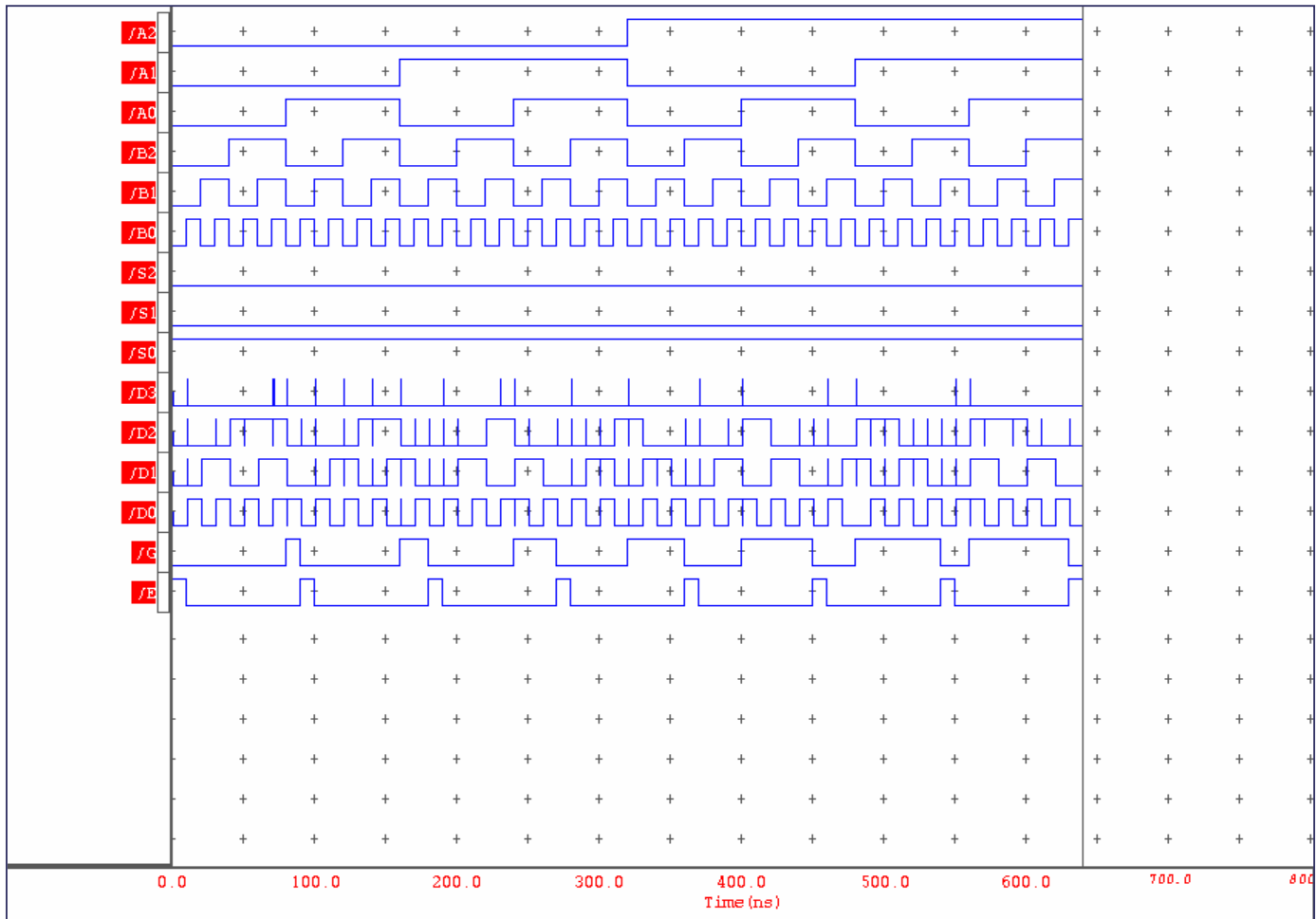


Figure 34: “2181” ALU PROJECT: Simulation 2/8

“2181” ALU PROJECT: Simulation 3/8

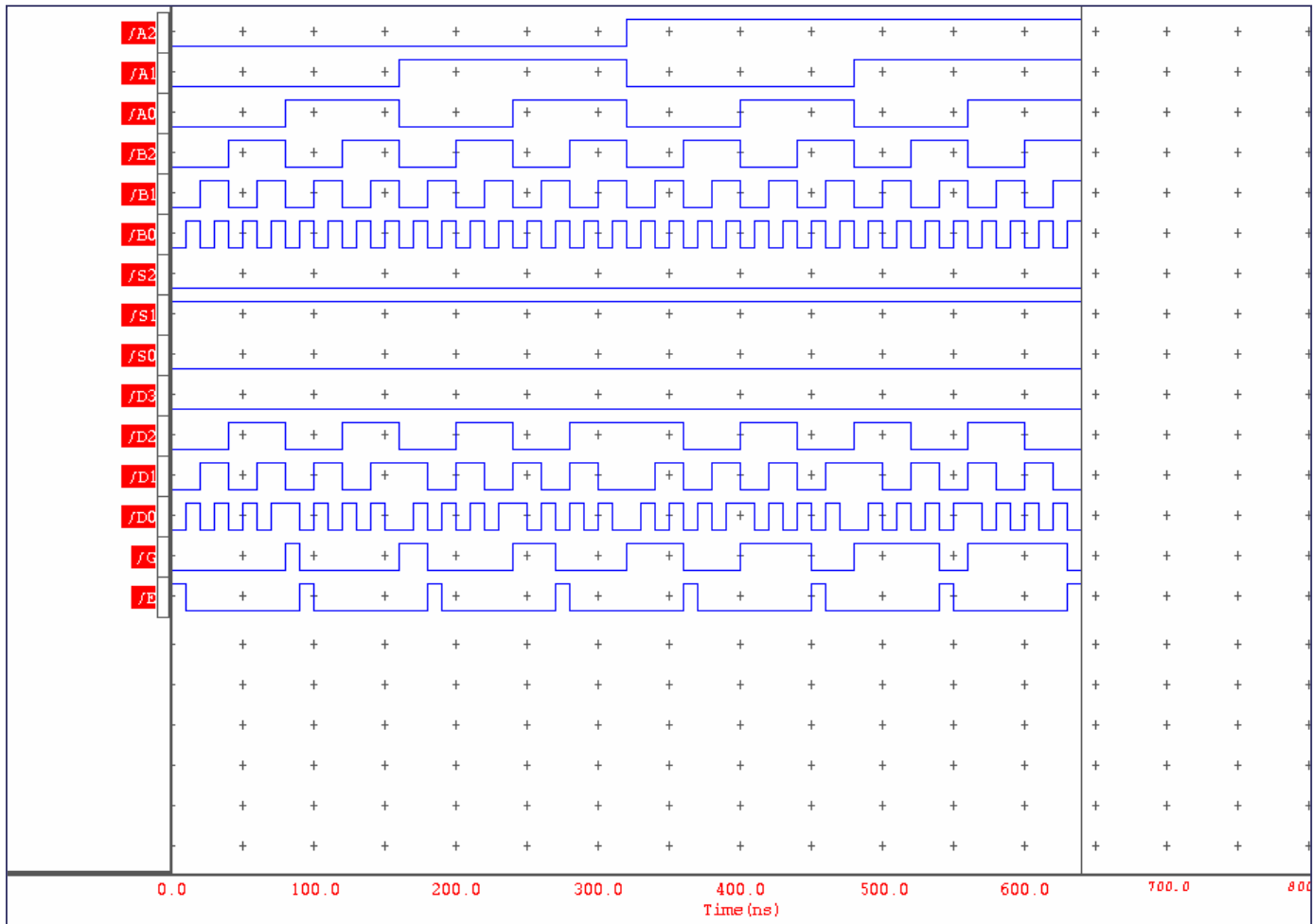


Figure 35: “2181” ALU PROJECT: Simulation 3/8

“2181” ALU PROJECT: Simulation 4/8

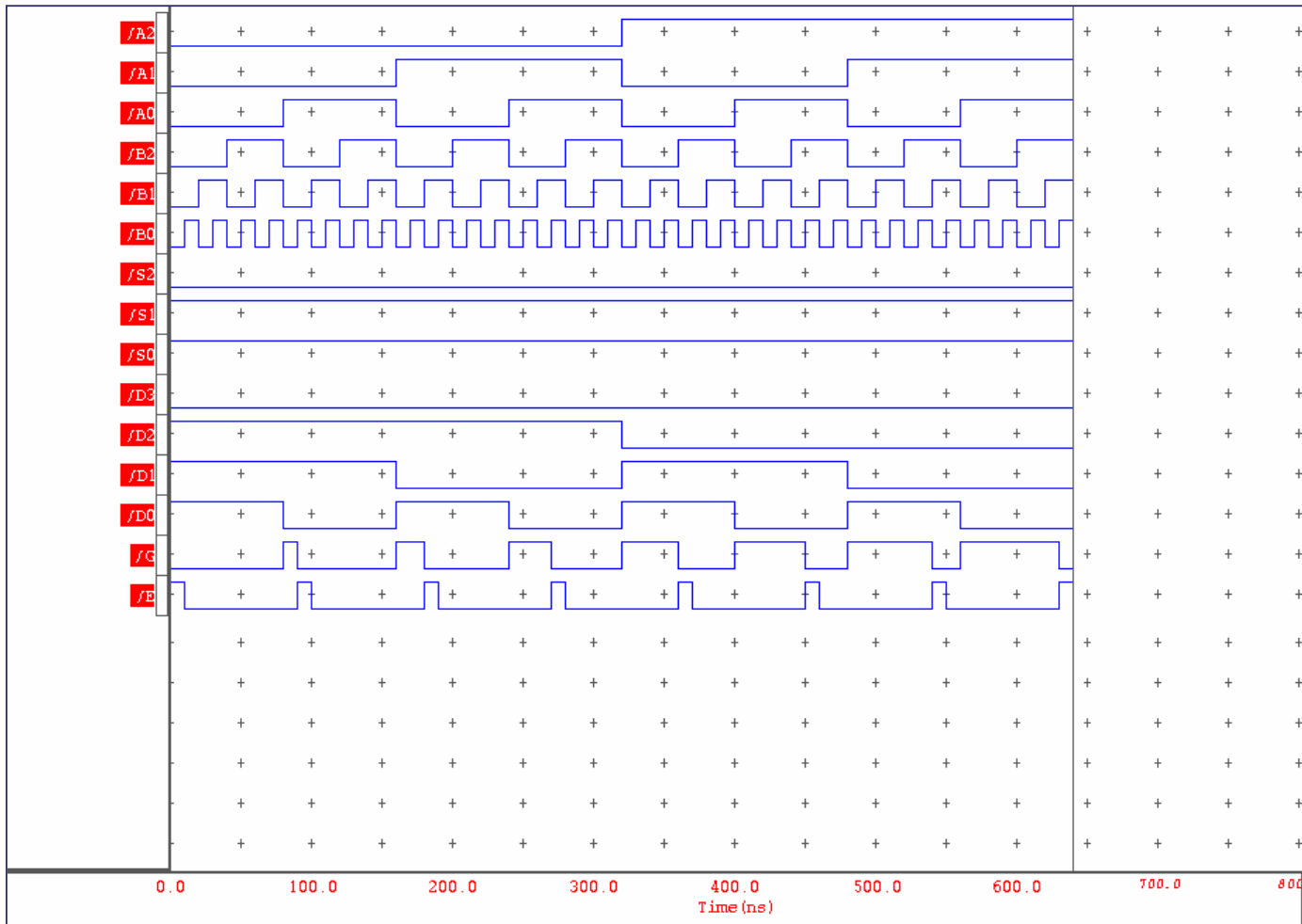


Figure 36: “2181” ALU PROJECT: Simulation 4/8

“2181” ALU PROJECT: Simulation 5/8

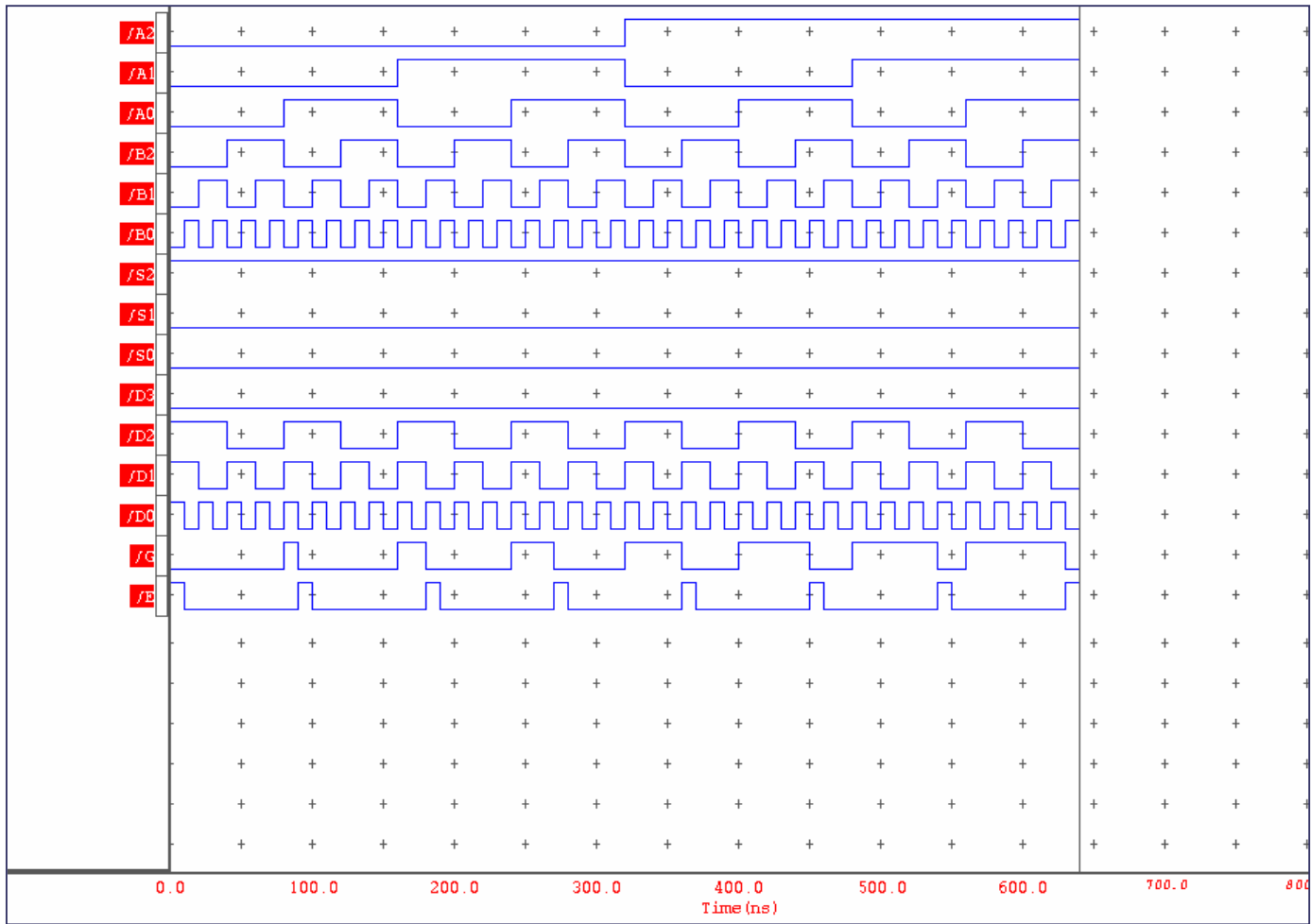


Figure 37: “2181” ALU PROJECT: Simulation 5/8

“2181” ALU PROJECT: Simulation 6/8

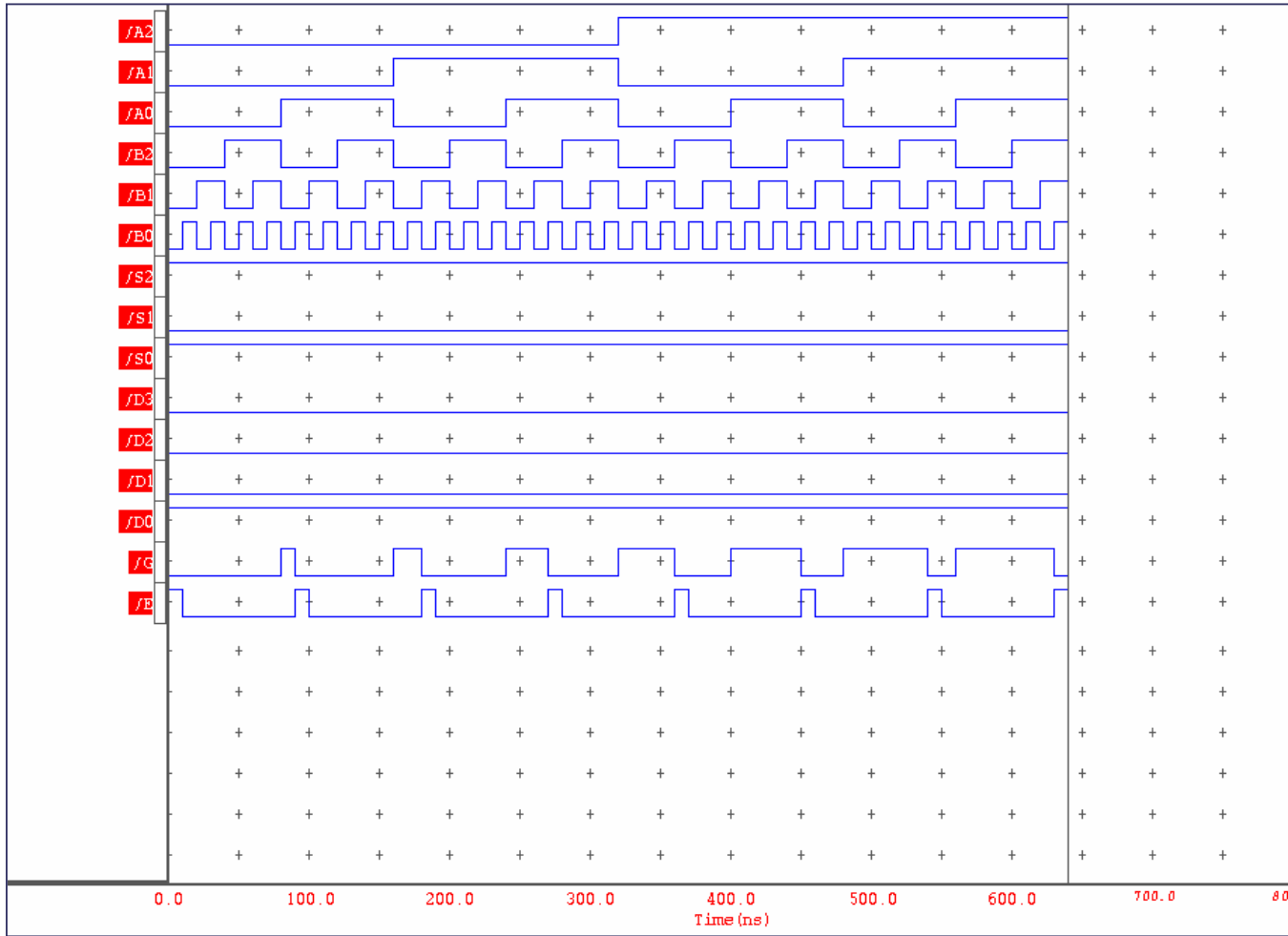


Figure 38: “2181” ALU PROJECT: Simulation 6/8

“2181” ALU PROJECT: Simulation 7/8

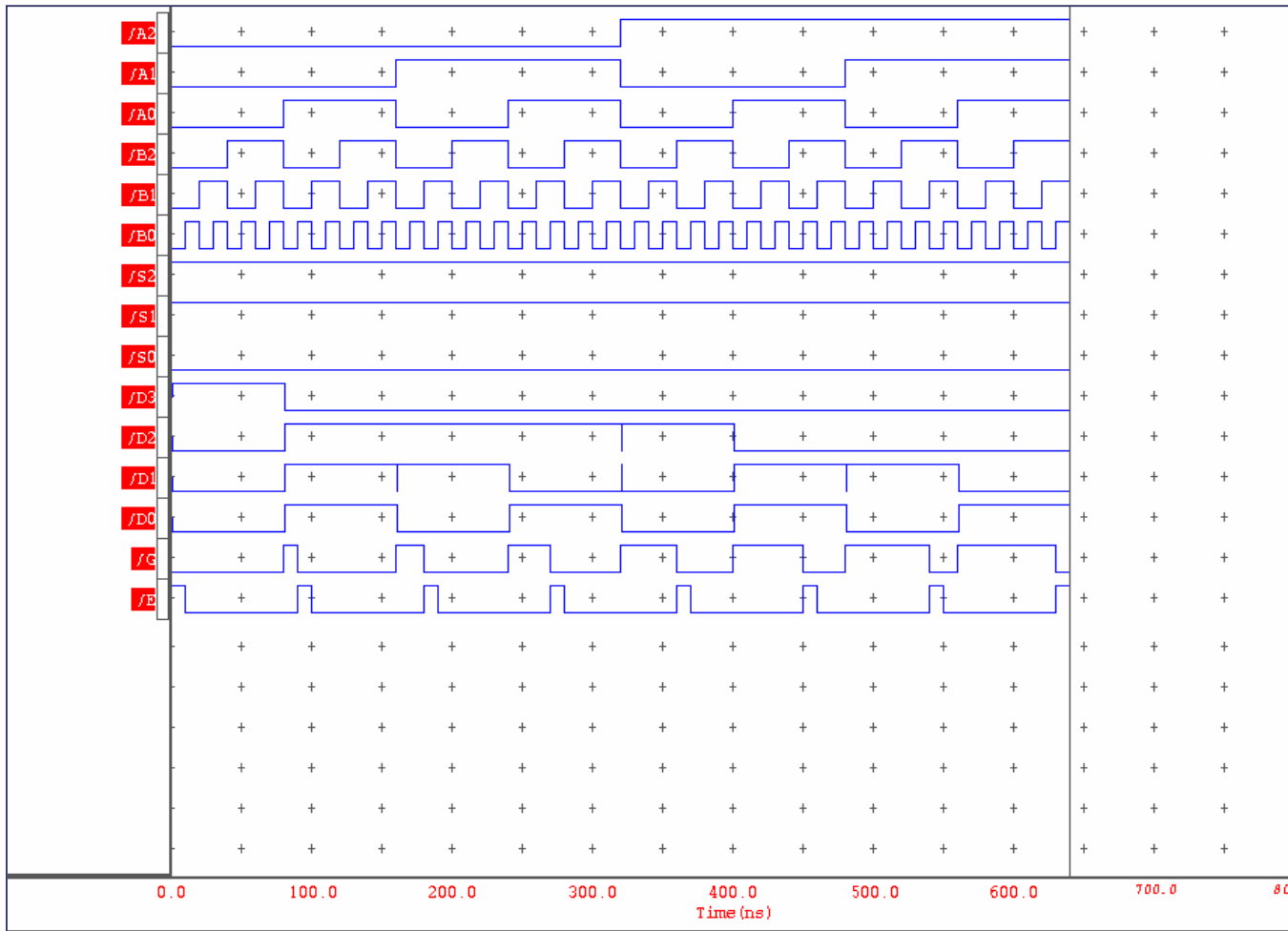


Figure 39: “2181” ALU PROJECT: Simulation 7/8

“2181” ALU PROJECT: Simulation 8/8

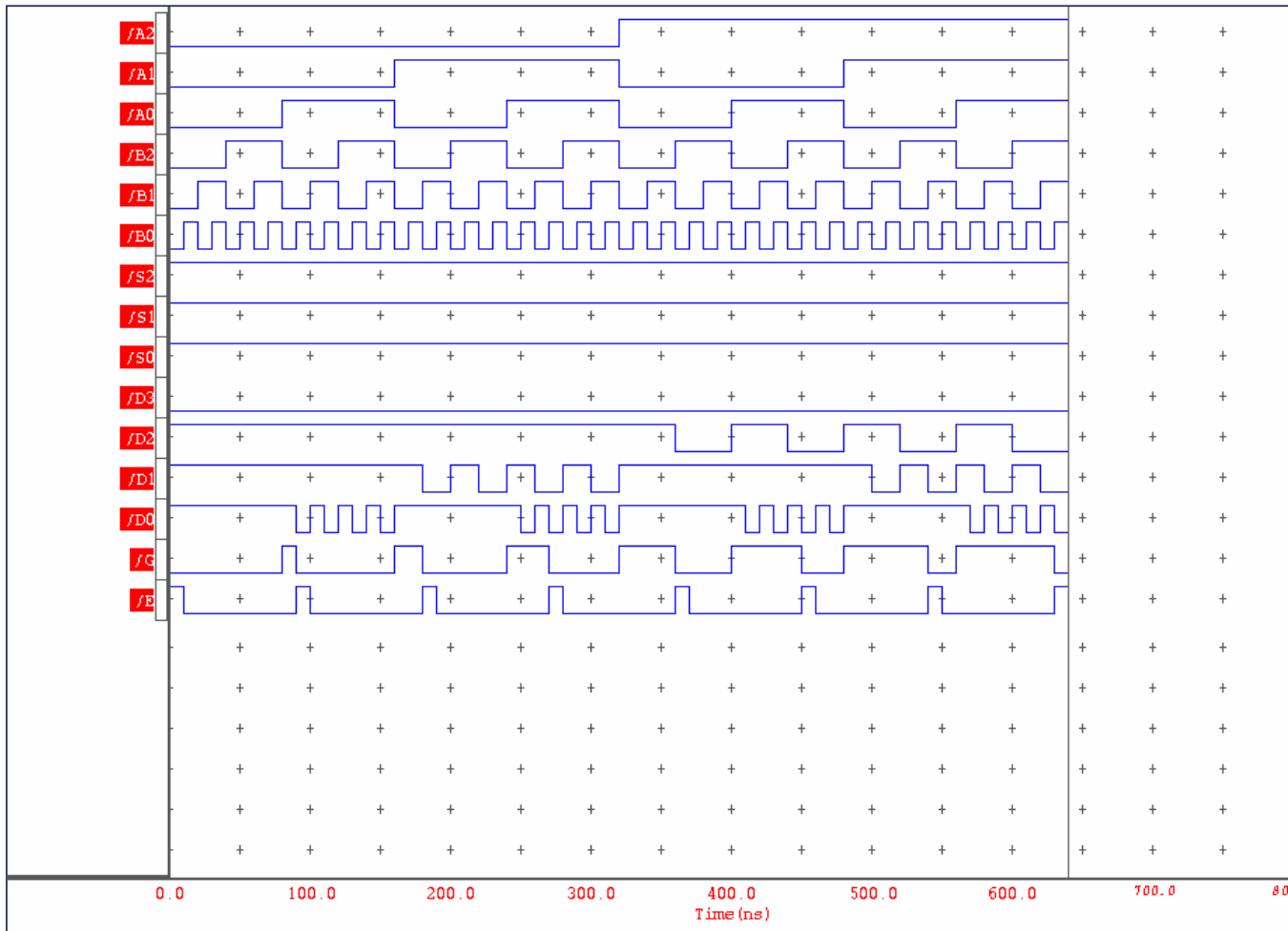


Figure 40: “2181” ALU PROJECT: Simulation 8/8

CONCLUSIONS

The results of the simulation matched the required criteria, and, in fact, the output of the “2181” ALU Project was consistent with the expected output; in other words, “2181” ALU Project worked properly.

All of the possible input and output combinations were simulated and tested, and no error was encountered; therefore the “2181” ALU Project is ready for a further implementation.