

Kushal Datta

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OBJECTIVE

Obtain a full time position in multi-core (MC) processor design and verification where I can effectively utilize my experience in hardware design, MC verification and simulation platform development, and design of energy-efficient high performance MC architectures to accomplish the company's goals.

EDUCATION

University of North Carolina, Charlotte, NC

Ph.D. in Electrical and Computer Engineering

May 2010

Dissertation: "Efficient exploration of shared memory heterogeneous Chip Multi-Threading design space, including intra-core and L2 cache memories, to maximize performance and minimize energy consumption. Network Processor (NeP) for Core Routers is a case study."

Honors: Expected dissertation defense March 2010

University of North Carolina, Charlotte, NC

MS in Electrical and Computer Engineering

2006

Project: "Automated design flow for diode-based Nano-fabrics"

Jadavpur University, KOLKATA, WB, INDIA

B.E. Honors in Computer Science and Engineering

2001

Areas of Concentration: Computer Architecture, Hardware Design, IC Design, Digital Logic

Honors: Passed with First Class Honors

AWARDS

Winner of OpenSPARC "Best submission that makes a substantial contribution to the OpenSPARC community" category of Community Innovation Contest 2008

2008

<http://www.opensparc.net/whats-new/2008-q3/community-innovation-awards-contest-winners.html>

Nallatech Research Fellowship, UNC Charlotte

2005 – 2008

RELATED EXPERIENCE

OpenSPARC Team, Sun Microsystems, Inc, Santa Clara, CA

Graduate Student Intern

Feb 2007 – Aug 2007

Provide as needed editorial support remotely, including developmental and copy editing of their internal online and printed documentation.

IBM India, Kolkata, WB, India

SAP Technical Consultant

2002 -2004

Two years and 4 months of experience as SAP Technical Consultant in IBM India, involving estimation, system analysis, design, testing, implementation and support of application software.

Responsibilities included

- Estimation and preparation of Functional and Technical Specs
- System Analysis and Test Problem Reports (TPR) solutions.
- Design, Construction, Testing of ABAP modules and mentoring junior developers
- Developing high complexity objects
- Leading the Control Programs Developing Team.

IIT Kharagpur, Kharahpur, WB, India

Junior Research Assistant

2001-2002

Design and development of Binary-Decision Diagram based synthesizer and mapping algorithms in Low Power Circuits and Systems project sponsored by Intel, USA.

SKILLS AND COMPETENCIES

HDL Simulation Tools: Modelsim SE/PE, Synopsis Scirocco/ VirSim, eProduct Designer (Mentor Graphics), GEMS, Sparc Architecture Simulator (SAM-T1/T2)
Synthesis Tools: Cadence Physically Knowledgeable Synthesis Tool, Xilinx Synthesis Tools
HDL: VHDL, Verilog
Assembly: SPARCV9 assembly
Languages: C/C++, JAVA, Perl, Shell Script, TCL, PHP, SPARCV9 Assembly
Operating Systems: Unix, Linux (Fedora), Solaris10, Windows

RESEARCH INTERESTS

- **Current Research:**
 - ❖ Development of parameterized multi-core simulation platforms to study Energy-Performance-Area of Chip Multi-Threading (CMT) multi-core architectures
 - ❖ In-depth analysis of energy/power consumption of CMT processors and development of energy/power models
 - ❖ Detailed analysis of shared memory contention and its effects on CMT performance
 - ❖ Efficient exploration of CMT design space including intra-core and L2 cache memories, to maximize performance and minimize energy consumption
 - ❖ Use our architecture exploration techniques to design energy efficient embedded processors.
 - **Parallel Benchmarks for evaluation of Multi-core Architectures**
 - **Parallel multi-threaded architectures**
 - **Automated Hardware-controlled Power-saving mechanisms**
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PUBLICATIONS AND PAPERS

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1. *Submitted:* "A Simulation Framework for studying Hardware-controlled Power Management Strategies in Embedded Multi-Core Network Processors", K. Datta, A. Mukherjee, Y. Liu, B. Joshi and A. Ravindran, Journal of Low Power and Electronica, 2009.
 2. *Submitted:* "CASPER: A SPARCV9-based Cycle-Accurate Chip Multi-Threaded Architecture Simulator for Performance, Energy and Area Analysis", K. Datta, A. Mukherjee, G. Cao, J. Byun, A. Ravindran, B. Joshi and Durgam Vahia, 24th IEEE International Parallel & Distributed Processing Symposium, Atlanta, 2010.
 3. *Book Chapter:* "Chapter 10: Hardware Techniques for Autonomous Power Saving in Embedded Many-Core Processors", Multicore Embedded Systems, September 2010.
 4. *Poster Presentation:* "A Parallel Power Flow Solver based on the Gauss-Seidel method on the IBM Cell/B.E", J. Byun, K. Datta, A. Ravindran, A. Mukherjee, B. Joshi and David Chassin, Nov. 2009, Proceedings of SuperComputing Conference 2009.
 5. "Performance Analysis of Coarse-grained Parallel Genetic Algorithms on the multicore Sun UltraSPARC T1", J. Byun, K. Datta, A. Mukherjee, A. Ravindran and B. Joshi, IEEE Southeast Con 2009 (Atlanta, GA)
 6. " Reconfigurable Computing Cluster (RCC) Project: Investigating the Feasibility of FPGA-Based
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- Petascale Computing", Ron Sass, Will Kritikos, Andrew Schmidt, Srinivas Beeravolu, Parag Beeraka, K. Datta, David Andrews, Richard Miller and Daniel Stanzione, Jr., Apr. 2007, Proceedings of Field Programmable Custom Computing Machines 2007.
7. *Poster Presentation*: "RBoot: A Virtual FPGA Laboratory", K. Datta and Ron Sass, Apr 2007, Proceedings of Field Programmable Custom Computing Machines 2007. (Poster Presentation)
 8. "Automated design flow for diode-based nanofabrics", K. Datta, A. Mukherjee, and A. Ravindran, 2006, J. of Emerg. Technol. Comput. Syst. 2, 3 (Jul. 2006), 219-241. DOI=<http://doi.acm.org/10.1145/1167943.1167946>
 9. "Routing for Reliability in Molecular Diode-based Nanofabrics", K. Datta, A. Mukherjee and A. Ravindran, Proceedings of the 8th Military and Aerospace Programmable Logic Device International Conference, September 2005.
 10. "The Wireless Sensor Tissue: A Network of Wireless Sensor Nodes using Cellular Mechanisms for Autonomous Distributed Fault Tolerance", K. Datta, J. Bolano, A. Mukherjee, A. Ravindran, Proceedings of the IEEE 15th North Atlantic Test Workshop 2006.
 11. "A Biology-inspired Self-Repairable Distributed Fault Tolerant Design Methodology for Highly Available Systems with Efficient Redundancy Insertion Technique", K. Datta, R.K. Karanam, J.H. Byun, A. Mukherjee, A. Ravindran, Proceedings of the IEEE 15th North Atlantic Test Workshop 2006.
 12. *Invited Talk*: "CMT Architecture Research Framework", K. Datta, 2008, Validation Summit 2008, Santa Clara, California
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TEACHING EXPERIENCE

Teaching Assistant – to Professor Fred Esenwein

Jan 2004 – Current

Taught the following undergraduate laboratory courses:

1. Instrumentation and Networks
 2. Logic and Networks
 3. Digital Design
 4. Systems and Electronics
 5. Electromagnetic and Electronic Devices
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MEMBERSHIPS

Phi Kappa Phi - American Honor Society of outstanding students who rank in the top 10% of their class and have achieved scholarly distinction

REFERENCES

Arindam Mukherjee

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Dr. Mukherjee is my Ph.D. Dissertation Advisor

Arun Ravindran

Phone: (704)-687-8427

Email: aravindr@uncc.edu

Dr. Ravindran is a member of my dissertation committee.

Bharat S. Joshi

Phone: (704)-687-8410

Email: bsjoshi@uncc.edu

Dr. Joshi is a member of my dissertation committee.