

Assignment 4

In this assignment we develop a Verilog A model of a comparator and a circuit realization of the Cho dynamic latched comparator in $0.5\mu\text{m}$ CMOS.

VerilogA comparator

Construct a VerilogA model of a comparator with $V_{DD} = 1.5$, $V_{SS} = -1.5$ and an offset of 200mV . Verify the operation of the comparator by a DC sweep of the input voltage between $-1\text{V} - 1\text{V}$.

Also examine the comparator model available in `ahdlLib`. Here the comparator is modeled as a high gain amplifier using a \tanh relation.

Cho comparator

Design and simulate the Cho differential dynamic latched comparator discussed in class at transistor level. Use the following parameters $V_{DD} = 1.5\text{V}$, $V_{SS} = -1.5\text{V}$, $V_{ref+} = 0.5\text{V}$, $V_{ref-} = -0.5\text{V}$, $\Phi_{latch} = 100\text{ KHz}$, $V_{trip} = 0.125\text{V}$. Size the transistors to have minimum possible geometry.

- Verify the operation using DC inputs of 0 , $+200\text{mV}$, -100mV
- A sine input of amplitudes 120mV and 130mV with $f_{in} = 10\text{ KHz}$.
- Simulating offsets: Let's assume that the comparator offset voltage is between -250mV to 250mV and we would like to measure offsets of at least 10mV . To do this, apply a differential ramp (use the `vpwl` source from `NCSU_Analog_Parts`) from -250mV to 250mV . To ensure that the offset is measured to the required accuracy, the input should not change by more than 10mV during a clock period. The ramp slope is, therefore, $10\text{mV}/10\mu\text{s} = 1000\text{ V/s}$ i.e. the ramp is applied for duration of 0.5 ms in the above example. Use a simulation step of $1\mu\text{s}$. Now apply a 10% mismatch between devices `M2` and `M3` of the Cho comparator (see Lecture 4 for device numbers). Simulate the trip point of the comparator and determine the offset. Repeat the simulations for a mismatch of 10% between `M5` and `M6`. What do you conclude?