

Arun Ravindran, Ph.D.

Assistant Professor, Electrical and Computer Engineering
The William States Lee College of Engineering, University of North Carolina at Charlotte
Ph: 704-687-8427 Fax: 704-687-4762 email: aravindr@uncc.edu
URL: <http://www.ece.uncc.edu/~aravindr>

EDUCATION

- § Ph.D. 2003 The Ohio State University (Columbus, Ohio). Electrical Engineering
- § M.S. 2000 The Ohio State University (Columbus, Ohio). Physics
- § M.Eng. 1997 Birla Institute of Technology and Science (Pilani, India). Microelectronics
- § B.Eng. 1996 Birla Institute of Technology and Science (Pilani, India). Instrumentation

PROFESSIONAL EXPERIENCE

- § ASSISTANT PROFESSOR: Department of Electrical and Computer Engineering. UNC-Charlotte. Teaching and research in electrical and computer engineering, with research interests in high performance computing, computer architecture, low power analog and mixed signal design, and digital microfluidics. (August 2003-present)
- § RESEARCH ASSISTANT, The Ohio State University, Department of Electrical Engineering. (Analog and Mixed signal design) (2002-2003)
- § TEACHING ASSISTANT, The Ohio State University, Departments of Electrical Engineering, Mathematics and Physics (1998-2002)
- § DESIGN ENGINEER, IBM (1998)

PUBLICATIONS

Journals

1. S. Datta, B. Joshi, A. Mukherjee, and A. Ravindran, "Efficient Testing and Diagnosis of Digital Microfluidic Biochips," Accepted for publication in the ACM Journal on Emerging Technologies in Computing System.
2. R. Karanam, A. Ravindran, and A. Mukherjee, "A Stream Chip-multiprocessor for Bioinformatics", ACM SIGARCH Computer Architecture News, Volume 36, Issue 2, pp. 2 – 9, May 2008
3. S. Tucker, A. Ravindran, C. Wichman, and A. Mukherjee, "Design Techniques for Micro-Power Algorithmic Analog-to-Digital Converters", Journal of Low Power Electronics, Vol. 3., pp. 1 - 10, April 2007.
4. D. Davids, S. Datta, A. Mukherjee, B. Joshi and A. Ravindran, "Multiple Fault Diagnosis in Digital Microfluidic Biochips", ACM Journal on Emerging Technologies in Computing Systems, vol. 2, no. 4, pp.1–15, October 2006.
5. S. Mohan, A. Ravindran, D. Binkley and A. Mukherjee, "Power Optimized Design of CMOS Programmable Gain Amplifiers", Journal of Low Power Electronics, Vol. 2, No:2, pp. 259-270, August 2006.
6. K. Datta, A. Mukherjee and A. Ravindran, "Automated Design Flow for Diode based Nanofabrics", ACM Journal of Emerging Technologies in Computing Systems, vol, 2, no.3, pp. 219-241, July 2006.
7. R. Karanam, A. Ravindran, A. Mukherjee, C. Gibas, and A. Wilkison, "Using FPGA-based Hybrid Computers for Bioinformatics Applications", XCell Journal, Issue 58, Third Quarter, 2006
8. K. Regester, J. Byun, A. Mukherjee and A. Ravindran, "Implementing Bioinformatics Algorithms on Nallatech-configurable Multi-FPGA Systems", Xcell Journal., pp. 100-103 Second Quarter, 2005.

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9. A. Ravindran, E. Vidal, S. Yoo, K. Ramarao and M. Ismail, "A Differential Current Mode Variable Gain Amplifier with a Digital dB-linear Gain Control", Journal of Analog Integrated Circuits and Signal Processing, Kluwer Academic Publishers, Vol. 38, Issue 2-3, pp. 161-174, February 2004.*
10. H. Elwan, A. Ravindran and M. Ismail, "A CMOS Low Power Baseband Chain for a GSM/DECT Multi-standard Receiver", IEE Proceedings: Circuits, Devices, and Systems, Vol. 149, Issue 5, pp. 337-347, Oct. 2002.*
11. A. Ravindran, K. Ramarao, E. Vidal and M. Ismail, "Compact Low-voltage Four Quadrant CMOS Current Multiplier", Electronic Letters, Volume: 37 Issue: 24, 22 Nov. 2001, pp. 1427-1428.*

Conferences

1. A. Ravindran, and D. Burns, "A multi-threaded DNA Tag/Anti-tag Library Generator for Multicore platforms", Accepted, IEEE Symposium on Computational Intelligence in Bioinformatics and Computational Biology, March, 2009.
2. A. Ravindran, A. Mukherjee, and P. Tolley, "An Undergraduate Computer Engineering Educational Framework for using Field Programmable Gate Arrays as Efficient Hardware Accelerators", Conference of Course, Curriculum and Laboratory Improvement Program, Aug 14-15, 2008.
3. Daniel Davids, Bharat Joshi, Arindam Mukherjee, and Arun Ravindran, "A Fault Detection and Diagnosis Technique for Digital Microfluidic Biochips," IEEE International Mixed-Signals, Sensors, and Systems Test Workshop, June 18-20, 2008.
4. R. Karanam, A. Ravindran and A. Mukherjee, "A Stream Chip Multiprocessor for Bioinformatics", Workshop on Design, Analysis and Simulation of Chip Multiprocessors, December, 2007.
5. Bharat Joshi, Arindam Mukherjee, and Arun Ravindran, "Highly Dependable SCADA Systems," National Workshop on Beyond SCADA: Networked Embedded Control for Critical Physical Systems, November 2006.
6. J. Byun, R. Karanam, A. Ravindran, A. Mukherjee and B. Joshi, "Fault Tolerant Techniques for I/O Bound High Performance Systolic Arrays on SRAM FPGAs", MAPLD, September 2006.
7. K. Datta, J. Bolano, O. Eruotor, Y. Nerie, A. Mukherjee, A. Ravindran, "The Wireless Sensor Tissue: A Network of Wireless Sensor Nodes using Cellular Mechanisms for Autonomous Distributed Fault Tolerance", North Atlantic Test Workshop May 10-12, 2006.
8. Kushal Datta, Ravi Kiran Karanam, Jong-Ho Byun, Arindam Mukherjee, Bharat Joshi, and Arun Ravindran, "A Biology-inspired Distributed Fault Tolerant Design Methodology for Highly Available Systems with Efficient Redundancy Insertion Technique," North Atlantic Test Workshop, May 10-12, 2006.
9. A. Ravindran and S. Mohan, "A Low Input Impedance Fully Differential CMOS Transresistance Amplifier using Cascode Regulation", IEEE CICC, September 2005.
10. C. Wichman, S. Tucker and A. Ravindran, "A Micropower OTA for Digitally Calibrated Algorithmic ADCs", 48th IEEE MWSCAS, August 2005.
11. J. Bolano, J. Johnson, A. Wood, A. Mukherjee, H. Hilger and A. Ravindran, "Real Time Wireless Remote monitoring of Methane Flux in Landfills", INCEED, July 2005.
12. A. Yamazaki, A. Ravindran, O. Akgun and M. Ismail, "An Active-RC Reconfigurable Lowpass-polyphase Tow-Thomas Biquad Filter", 47th IEEE MWSCAS, July 2004.
13. A. Savla, A. Ravindran and J. Leonard, "A Novel Queuing Architecture for Background Calibration in Pipelined ADCs", IEEE ISCAS, May 2004.
14. A. Ravindran, A. Savla and J. Leonard, "Digital Error Correction and Calibration of Non-linearities in a Pipelined ADC", IEEE ISCAS, May 2004
15. Y. Yoo, A. Ravindran and M. Ismail, "A Low Voltage CMOS Transresistance-based Variable Gain Amplifier", IEEE ISCAS, May 2004.*
16. A. Savla, A. Ravindran and M. Ismail, "A Reconfigurable Low-IF/Zero-IF Receiver Architecture for Multi-Standard Wide Area Wireless Networks", IEEE ICECS 2003, pp. 934-937, December 2003.*
17. A. Savla, A. Ravindran, J. Leonard and M. Ismail, "System Analysis of a Multi-standard Wireless Direct Conversion Receiver", 45th IEEE MWSCAS Conference, August 2002.*
18. A. Ravindran, A. Savla, I. Younus and M. Ismail, "A 0.8V CMOS Filter based on a Novel Low Voltage Operational Trans-resistance Amplifier", 45th IEEE MWSCAS, August 2002.*
19. A. Savla, A. Ravindran and M. Ismail, "A Reconfigurable Low Power Pipeline ADC for Multi-standard Wireless Applications", IEE-Japan, Analog VLSI Workshop, September 2002.*

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20. A. Ravindran, E. Vidal and M. Ismail, "A Digitally Generated Exponential Function for dB-linear CMOS Variable Gain Amplifiers", 14th International Conference on Digital Signal Processing, July 2002.*

Book Chapter

1. B. Joshi, A. Mukherjee, and A. Ravindran, "Architectural Optimizations under Fault Conditions for Emerging Digital Microfluidic Biochips", Book chapter, VLSI Circuits for Biomedical Applications, Kris Iniewski, Editor, Artech House, 2008.
2. M. I. Younus, A. Ravindran, A. Savla and M. Ismail, "A reconfigurable Baseband Chain for 3G Wireless Receivers", Chapter 3, Wireless Communication Circuits and Systems, Editor, Y. Sun, IEE Press, 2003.*

Patents

- A. Mukherjee, and A. Ravindran, "A Methodology for Scheduling, Partitioning, and Mapping Computational Tasks to Scalable High Performance Hybrid FPGA Networks", US Patent US 2005/027860

*Published as a graduate student at The Ohio State University

FUNDED PROJECTS

Total Funding: \$487,880 excluding departmental startup funds of \$25,000

1. **A. Ravindran (PI)** and A. Mukherjee, "Characterization of Electromagnetic Interference for a Pilot Broadband over Power Line Service", \$12,000, Duke Energy, 2004
2. **A. Ravindran (PI)**, "Architectures for Reconfigurable Bioinformatics Hardware Accelerators", \$6000, UNC-Charlotte Faculty Research Grant, 2005-2006
3. A. Mukherjee, **A. Ravindran (co-PI)** and K. Subramanian, "CRI: Field Programmable Gate Array (FPGA) based Hypercomputing Acceleration Platform for Bioinformatics", \$144,875, NSF, #0453916, 2005-2007.
4. A. Mukherjee, **A. Ravindran (co-PI)** and K. Subramanian, "REU-CRI: Field Programmable Gate Array (FPGA) based Hypercomputing Acceleration Platform for Bioinformatics", \$8000, NSF, #0453916, 2005-2007.
5. A. Mukherjee and A. Ravindran (**co-PI**), "Accelerating Bioinformatics Applications on Hybrid Computing Systems", \$30,000, Nallatech Inc., 2005-2008.
6. **A. Ravindran (PI)** and A. Mukherjee, "High Performance Powerflow Analysis", \$48,000 Pacific Northwest National Labs, 2007-2009
7. A. Mukherjee, **A. Ravindran (co-PI)** and B. Joshi, "A Practical CAD Approach for Optimizing Multi-Threaded Chip Multi-Processor Architectures", \$21,500, Sun Microsystems, 2007-2008
8. **A. Ravindran (PI)**, A. Mukherjee, and P. Tolley, "An Undergraduate Computer Engineering Educational Framework for Using Field Programmable Gate Arrays as Efficient Hardware Accelerators", \$150,000, NSF, 2007-2009.
9. I. Howitt, H. Hilger, **A. Ravindran (co-PI)**, A. Mukherjee, A. Willis and R. Guyer, "A Feasibility Study: Dynamic Predictive Maintenance System for Mitigating Sewer System Overflow", \$67,505, 2008.

TEACHING*

Recipient of the Williams States Lee College of Engineering Teaching Excellence at Undergraduate Level, 2008

Courses taught

1. ECGR 6157/8157 (CMOS Data Converters, Graduate)
2. ECGR 6090/8090 R01 (Multicore Computing, Graduate)
3. ECGR 3090/6090 (Analog System Design, Graduate/Undergraduate)
4. ECGR 4132/5132 (Analog IC Design, Graduate/Undergraduate)
5. ECGR 3131 (Fundamental of Semiconductors and Electronics, Undergraduate)

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6. ECGR 3132 (Electronics, Undergraduate)
7. ECGR 2111 (Network Theory – I, Undergraduate)
8. ECGR 2112 (Network Theory – II, Undergraduate)

*Teaching load of four courses per year

UNDERGRADUATE CURRICULUM DEVELOPMENT

Hardware acceleration using FPGAs (ECGR 4146): NSF funded course seeking to introduce undergraduate computer engineering students to high performance computing using Field Programmable Gate Arrays.

Analog System Design (ECGR 3090/6090): New course senior/beginning graduate course on board level analog system design. This course is designed for advanced undergraduate and beginning graduate students with a good background in electronics. The course presents topics in analog system design including design and analysis of filters, tuned amplifiers, oscillators, rectifiers and voltage regulators.

GRADUATE CURRICULUM DEVELOPMENT

CMOS Data Converters (ECGR 6157/8157): New graduate course for experienced analog, mixed-signal graduate students covering advanced topics in VLSI CMOS data converters. The course incorporates a design project where students are expected to design and layout an analog-to-digital converter. Successful designs will be fabricated in 0.5 μ m CMOS through MOSIS. Circuit simulation and system level modeling using Cadence and Matlab are used extensively throughout the course.

Multicore Computing (ECGR 6090.8090 R01): The course introduces graduate students to multicore processor architectures, parallel algorithms, thread programming, and performance characterization. Students are expected to complete an individual project implementing a computationally intensive algorithm on a commercial multicore platform.

GRADUATE STUDENTS

Primary advisor for

Ph.D.

1. Jong-Ho Byun "*High Performance Computing Techniques in Power Flow Analysis*", Expected date of graduation: Spring 2009
2. Changshu Zhang

M.S.

1. Christopher Wichman, "*Design of Low Voltage, Micropower Algorithmic Analog to Digital Converters*", Graduated in Spring 2005, Currently at Analog Devices Inc.
2. Srikanth Mohan, "*Transresistance Amplifier based Variable Gain Amplifiers*", Graduated in Fall 2005, Currently at Maxim Integrated Products Inc.
3. Chetan Vemula (Non-Thesis project), Graduated Fall 2006
4. Ravikiran Karanam, "*A Stream Multiprocessor Architecture for Bioinformatics Applications*", Graduated in Fall 2007, Currently at Qualcomm Inc.
5. Robert Crawford, "*Leakage Control Techniques in Low Voltage Switched-Opamp Circuits*", Expected to graduate in Fall 2008.
6. Vamsikrishna Parupalli
7. Sasa Cvijetic
8. Aby Kuruvilla

Arun Ravindran

9. Monil Neema

10. Anup Kulkarni

PROFESSIONAL SERVICE CONTRIBUTIONS

Departmental Service

- Department of Electrical and Computer Engineering Faculty Search Committee, Member, 2004-2005
- Membership of the ABET Circuits-electronics and Computer Engineering Focus Area Improvement Team (2003- Present).
- Member, Departmental Strategic Planning Committee.
- Active schedule advising of computer engineering students.
- Established the widely used Cadence™ computer aided design tools for integrated circuit design and am currently actively maintaining it.
- Involved in UNC-Charlotte/Western Carolina University collaboration through coordinating the simultaneous teaching of the sophomore course Networks – I on both campuses.
- Member, Departmental Outreach Committee 2006 – Present.
- Chair, Circuits and Electronics FAIT 2007- Present.
- Chair, ECE Faculty Associate Search Committee, 2008.
- Chair, EPIC Area Committee (Circuits and Electronics), 2008.

College Service

- Member, committee for the Lee COE Undergraduate Teaching Excellence Award.

University Service

- Alternate Representative, Faculty Curriculum Instruction Development, Academic Program Initiative Grants Committee (CID/AIP) (2006-2008)
- Primary Representative, Faculty Competitive Grants Committee (2008-2010)
- Graduate School Representative on the Ph.D. committee for Mr. Songtao Guo (Software and IS).
- Graduate School Representative on the Ph.D. committee for Ms. Mei Li (Mathematics)

External Service

- International Conference on Energy, Environment and Disasters, Session Chair for Environmental Monitoring and Site Characterization Techniques, Charlotte, 2005.
- IEEE Midwest Symposium on Circuits and Systems, Session Chair for Analog Circuits- Oscillators and PLLs, Cincinnati, 2005.
- Organized a NSF sponsored one day national faculty workshop on Introducing Reconfigurable Computing in the Undergraduate Computer Engineering Curriculum.
- Reviewer
 - IEE Proceedings on Circuits and Systems
 - Journal of Analog Integrated Circuits and Signal Processing
 - ETRI Journal of Information, Telecommunication and Electronics
 - IEEE Transactions on Circuits and Systems
 - IEEE International Conference on Circuits and Systems
 - IEEE Midwest Symposium on Circuits and Systems

HONORS AND AWARDS

- National Talent Search Scholarship, (India) 1992 to 1998.
- Hazel Brown Award for Teaching Excellence, The Ohio State University, 2000.
- Best Paper Award, IEE-Japan, Analog VLSI Workshop, 2002.
- Williams States Lee College of Engineering Teaching Excellence at the Undergraduate Level, 2008